

VM8G Block Diagram Intel Discrete GFX

VER : F3B

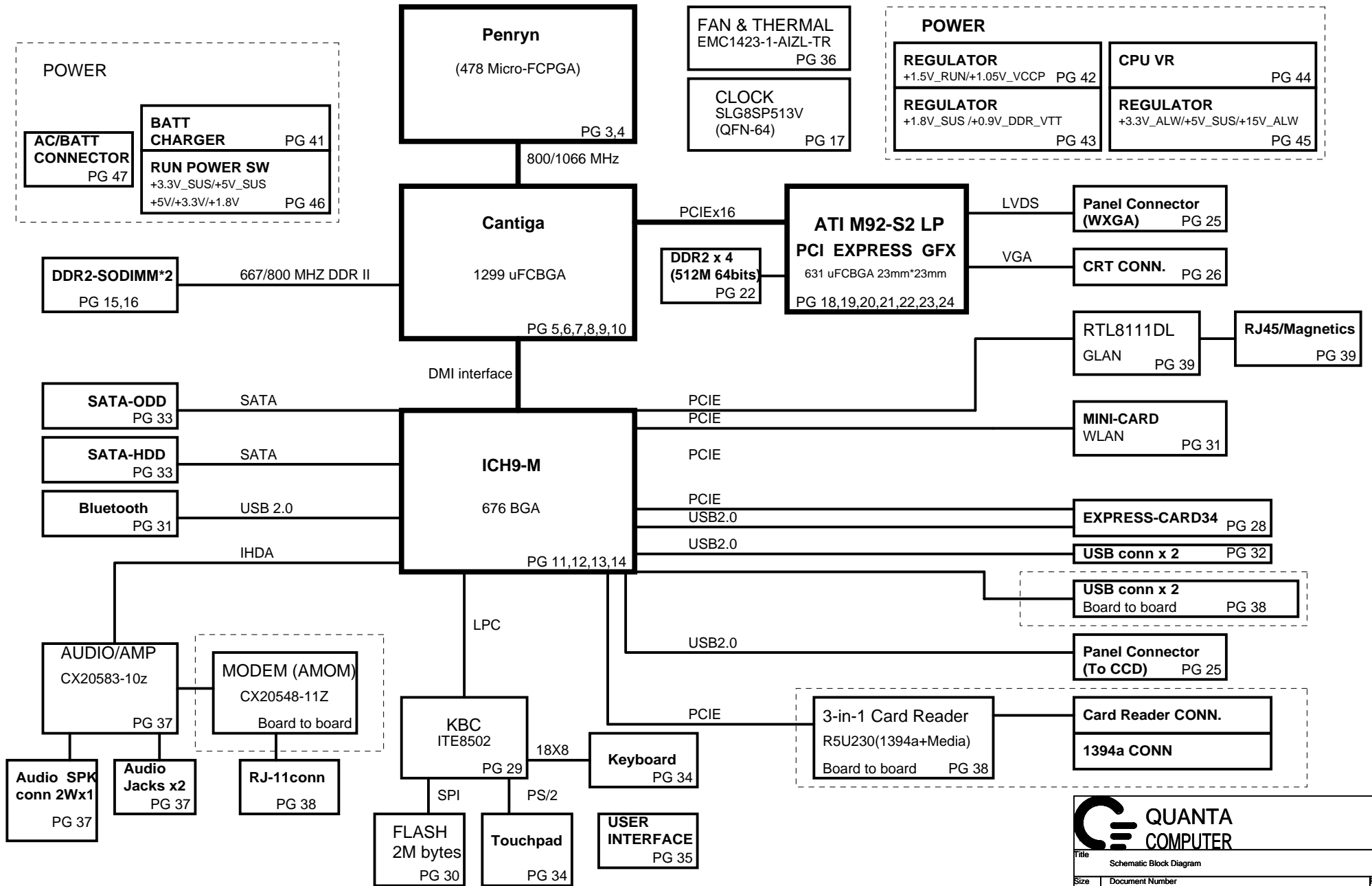



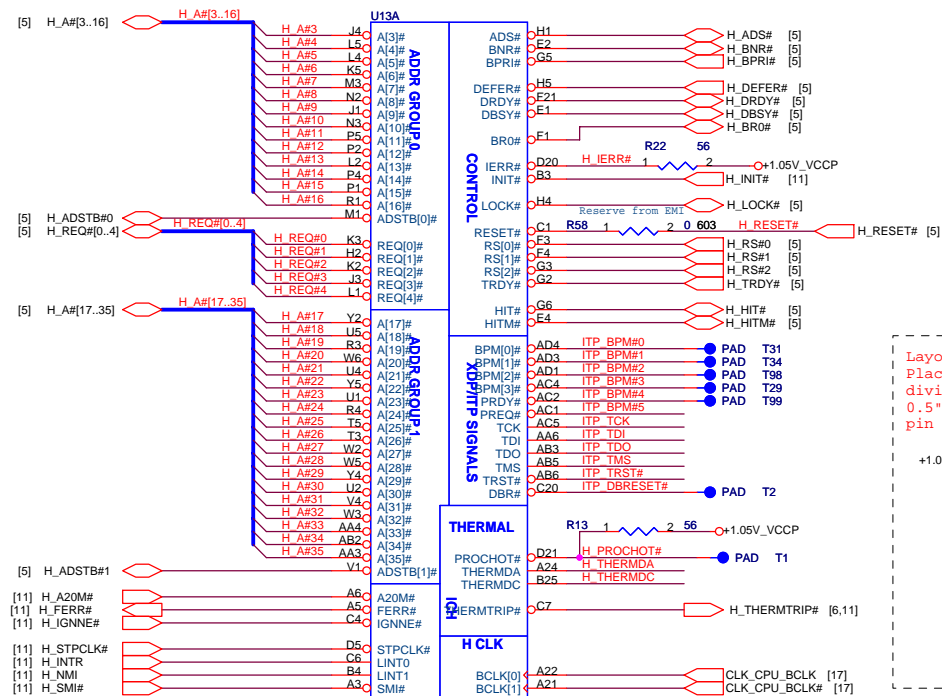
Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-24	M92-S2
25	LCD Conn.
26	CRT Conn
27	BLANK PAGE
28	Express Card
29	SIO (ITE8512)
30	FLASH/RTC
31	Mini Card / BT
32	USB
33	SATA Conn
34	TP / KEYBOARD
35	SWITCH /LED
36	FAN & Thermal
37	Audio CODEC(CX20583-10z)/Phone Jack
38	Module Board
39	LAN / TRANSFORM
40	BLANK PAGE
41	Charger (MAX8731A)
42	1.05VCCP / 1.5VRUJN
43	DDR2_1.8VSUS, 0.9V
44	CPU MAX17410 (2phase)
45	MAX17020 (+5.5V,+3.3V)
46	RUN Power Switch
47	DCIN,Batt
48	PAD& SCREW
49	VGA GFX CORE
50	EMI CAP
51	SMBUS BLOCK
52	Power Block Dianram

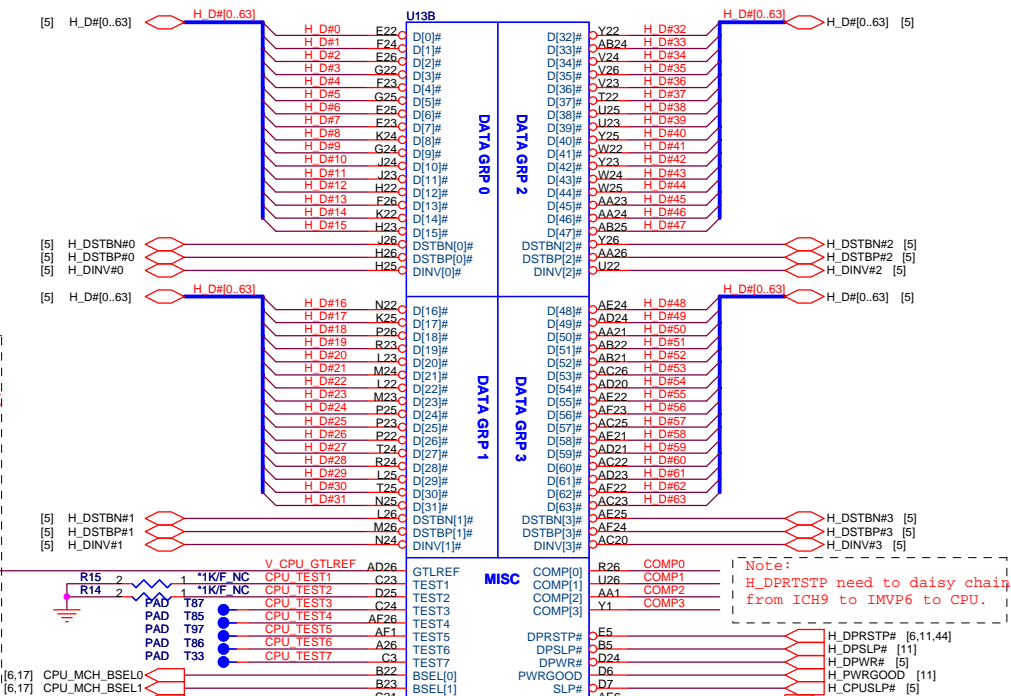
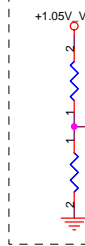
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,25,30,39,41,42,43,44,45,49,50	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,29,30	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,29,30,35,39,40,41,43,45,46,47	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	42,43,45,46,47,49	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	25,45,46	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	39	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,32,35,44,45,46,49,50	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,19,25,28,35,42,44,46,49	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,42,43,46,49	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,43,46	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,26,33,34,35,36,37,46,50	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,19,25,26,27,28,29,31,33,35,36,37,39,46,50	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,28,31,42,46,50	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,42,50	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,44	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	25	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	33	Module Power	MODC_EN#	
+5V_HDD	+5V	33	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	
+1.1V_GFX_PCIE	+1.1V	20	GFX PCIE POWER	GFX_RUN_ON	
+VCC_GFX_CORE	+0.9~+1.1	20,23,49	GFX CORE POWER	GFX_RUN_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



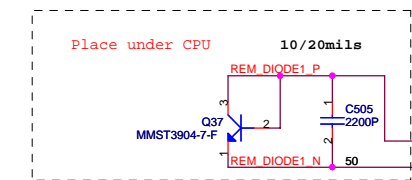
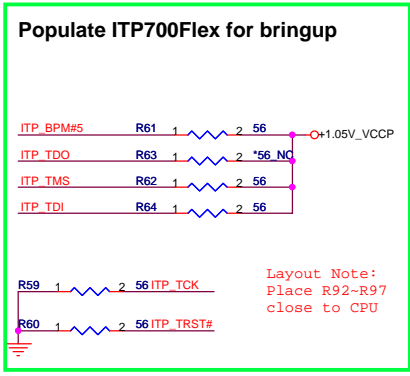
Layout Note:
Place voltage
divider within
0.5" of GTLREF
pin



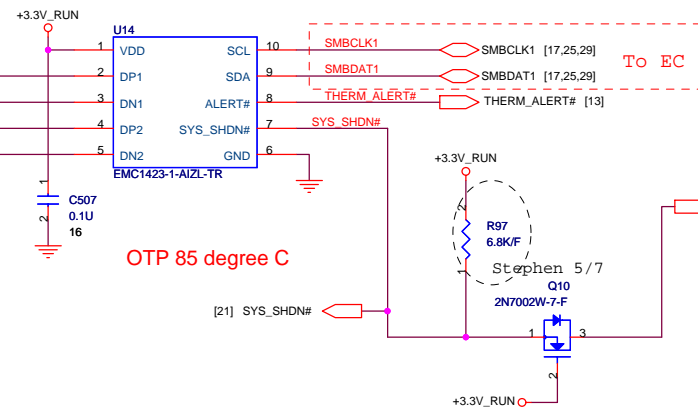
Note:
H_DPRTSTP need to daisy chain
from ICH9 to IMVP6 to CPU.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

Comp0,2 connect with Zo=27.4ohm,
Comp1,3 connect with Zo=55ohm,
make those traces length shorter than 0.5".
Trace Comp0,2 should be 18-Mil Wide.
Trace Comp1,3 should be 5-Mil Wide.



Cap should close to thermal IC



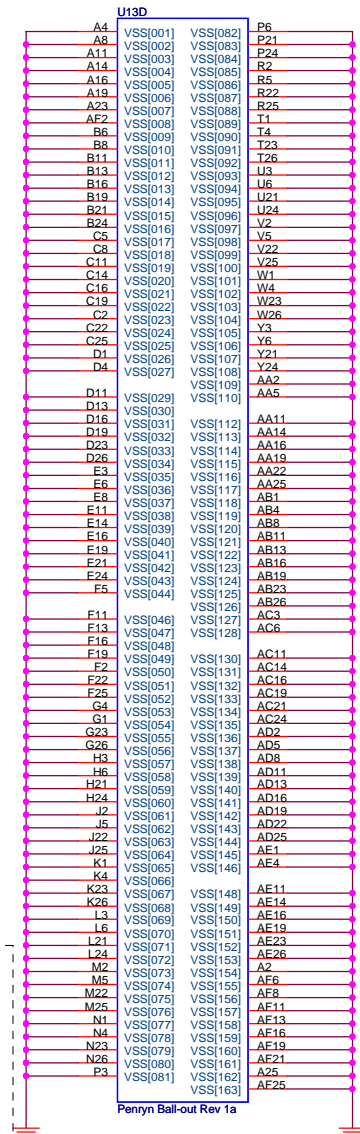
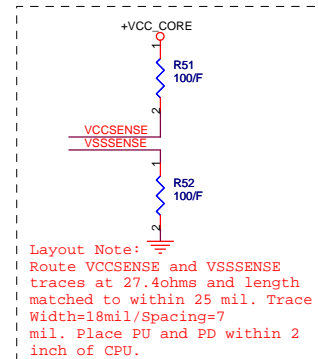
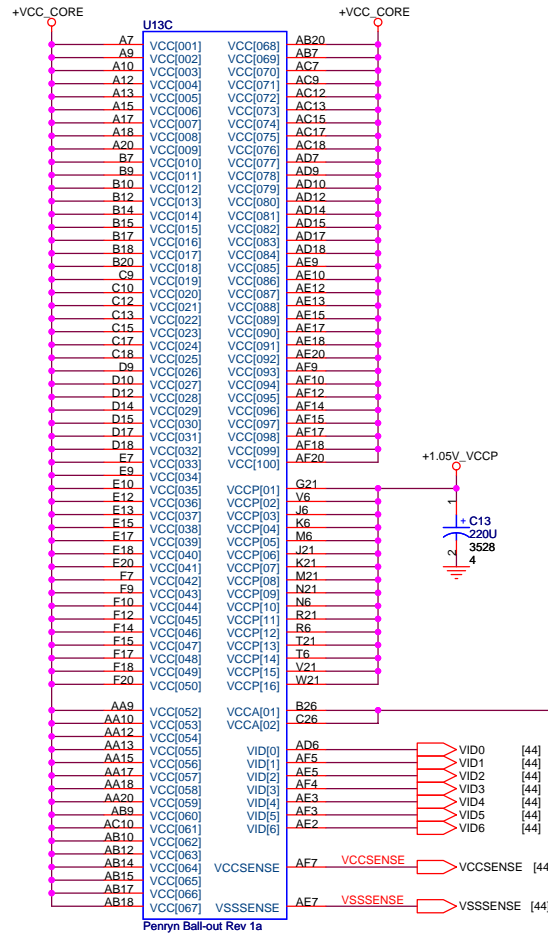
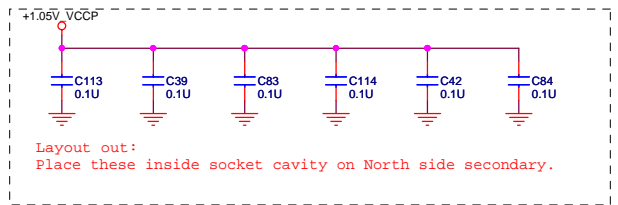
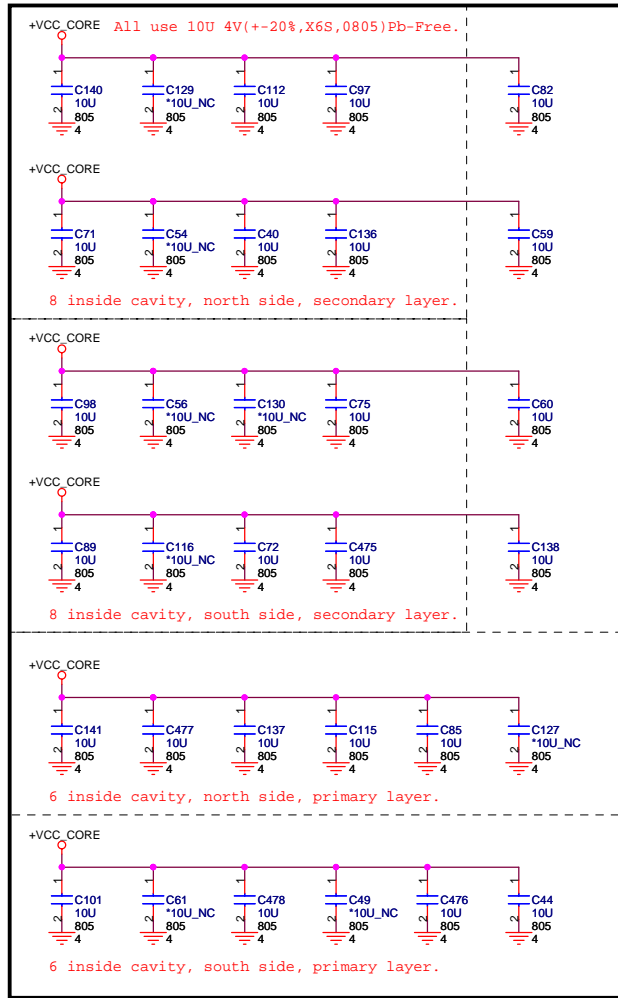
OTP 85 degree C

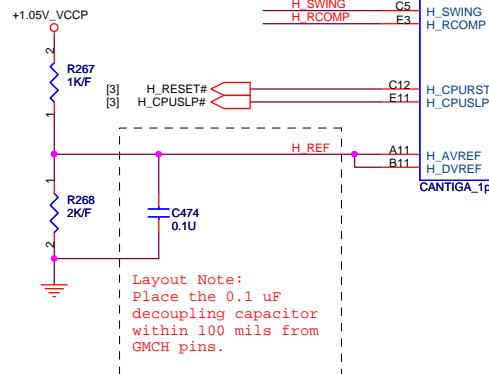
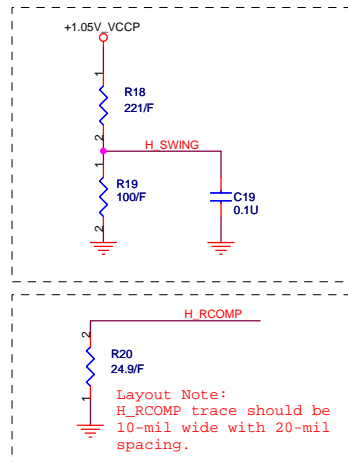
**QUANTA
COMPUTER**

File: Penryn Processor (HOST BUS)

Size: Document Number VM8G Rev 1B

Date: Tuesday, June 02, 2009 Sheet 8 of 53





U12A

H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	F8	H_D#_2
H_D#3	E6	H_D#_3
H_D#4	G2	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M1	H_D#_11
H_D#12	J1	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	P2	H_D#_16
H_D#17	L2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	N9	H_D#_19
H_D#20	L6	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N6	H_D#_25
H_D#26	N8	H_D#_26
H_D#27	N8	H_D#_27
H_D#28	L7	H_D#_28
H_D#29	N10	H_D#_29
H_D#30	M3	H_D#_30
H_D#31	Y2	H_D#_31
H_D#32	AD14	H_D#_32
H_D#33	Y6	H_D#_33
H_D#34	Y10	H_D#_34
H_D#35	Y12	H_D#_35
H_D#36	Y14	H_D#_36
H_D#37	Y2	H_D#_37
H_D#38	W2	H_D#_38
H_D#39	AA8	H_D#_39
H_D#40	AA9	H_D#_40
H_D#41	AA11	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE9	H_D#_48
H_D#49	AE3	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AE3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	E16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35

H_ADS#	H12	H_ADS# [3]
H_ADSTB#_0	B16	H_ADSTB#0 [3]
H_ADSTB#_1	G17	H_ADSTB#1 [3]
H_BNR#	A9	H_BNR# [3]
H_BPRI#	E11	H_BPRI# [3]
H_BRQ#	G12	H_BRQ# [3]
H_DEFER#	E9	H_DEFER# [3]
H_DBSY#	B10	H_DBSY# [3]
HPLL_CLK	AH7	CLK_MCH_BCLK [17]
HPLL_CLK#	AH6	CLK_MCH_BCLK# [17]
H_DPWR#	H11	H_DPWR# [3]
H_DRDY#	H9	H_DRDY# [3]
H_HIT#	E12	H_HIT# [3]
H_HITM#	H11	H_HITM# [3]
H_LOCK#	C9	H_LOCK# [3]
H_TRDY#		H_TRDY# [3]

H_DINV#_0	J8	H_DINV#0 [3]
H_DINV#_1	L3	H_DINV#1 [3]
H_DINV#_2	Y13	H_DINV#2 [3]
H_DINV#_3	Y1	H_DINV#3 [3]

H_DSTBN#_0	L10	H_DSTBN#0 [3]
H_DSTBN#_1	M7	H_DSTBN#1 [3]
H_DSTBN#_2	AA5	H_DSTBN#2 [3]
H_DSTBN#_3	AE6	H_DSTBN#3 [3]

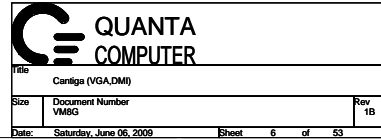
H_DSTBP#_0	L9	H_DSTBP#0 [3]
H_DSTBP#_1	M8	H_DSTBP#1 [3]
H_DSTBP#_2	AA6	H_DSTBP#2 [3]
H_DSTBP#_3	AE5	H_DSTBP#3 [3]

H_REQ#_0	B15	H_REQ#0 [3]
H_REQ#_1	K13	H_REQ#1 [3]
H_REQ#_2	E13	H_REQ#2 [3]
H_REQ#_3	B13	H_REQ#3 [3]
H_REQ#_4	B14	H_REQ#4 [3]

H_RS#_0	B6	H_RS#0 [3]
H_RS#_1	E12	H_RS#1 [3]
H_RS#_2	C8	H_RS#2 [3]

For EA test use

ET8	1	H_DSTBP#0
ET4	1	H_D#7
ET1	1	H_D#12
ET6	1	H_DSTBN#1
ET7	1	H_DSTBP#1
ET5	1	H_D#29
ET3	1	H_D#21
ET2	1	H_D#32



[15] DDR_A_D[0..63]

DDR A D0	AJ38	SA_DQ_0
DDR A D1	AJ41	SA_DQ_1
DDR A D2	AN38	SA_DQ_2
DDR A D3	AM38	SA_DQ_3
DDR A D4	AJ36	SA_DQ_4
DDR A D5	AJ40	SA_DQ_5
DDR A D6	AM44	SA_DQ_6
DDR A D7	AM42	SA_DQ_7
DDR A D8	AN43	SA_DQ_8
DDR A D9	AN44	SA_DQ_9
DDR A D10	AJ40	SA_DQ_10
DDR A D11	AT36	SA_DQ_11
DDR A D12	AN41	SA_DQ_12
DDR A D13	AN39	SA_DQ_13
DDR A D14	AJ44	SA_DQ_14
DDR A D15	AJ42	SA_DQ_15
DDR A D16	AV39	SA_DQ_16
DDR A D17	AY44	SA_DQ_17
DDR A D18	BA40	SA_DQ_18
DDR A D19	BD43	SA_DQ_19
DDR A D20	AV41	SA_DQ_20
DDR A D21	AY43	SA_DQ_21
DDR A D22	BA41	SA_DQ_22
DDR A D23	BC40	SA_DQ_23
DDR A D24	AY37	SA_DQ_24
DDR A D25	BD38	SA_DQ_25
DDR A D26	AV37	SA_DQ_26
DDR A D27	AT36	SA_DQ_27
DDR A D28	AY38	SA_DQ_28
DDR A D29	BB38	SA_DQ_29
DDR A D30	AV36	SA_DQ_30
DDR A D31	AW36	SA_DQ_31
DDR A D32	BD13	SA_DQ_32
DDR A D33	AJ11	SA_DQ_33
DDR A D34	BC11	SA_DQ_34
DDR A D35	BA12	SA_DQ_35
DDR A D36	AJ13	SA_DQ_36
DDR A D37	AV13	SA_DQ_37
DDR A D38	BD12	SA_DQ_38
DDR A D39	BC12	SA_DQ_39
DDR A D40	BB9	SA_DQ_40
DDR A D41	BA9	SA_DQ_41
DDR A D42	AJ10	SA_DQ_42
DDR A D43	AV9	SA_DQ_43
DDR A D44	BA11	SA_DQ_44
DDR A D45	BD9	SA_DQ_45
DDR A D46	AY8	SA_DQ_46
DDR A D47	BA6	SA_DQ_47
DDR A D48	AV5	SA_DQ_48
DDR A D49	AV7	SA_DQ_49
DDR A D50	AT9	SA_DQ_50
DDR A D51	AN8	SA_DQ_51
DDR A D52	AJ5	SA_DQ_52
DDR A D53	AJ6	SA_DQ_53
DDR A D54	AT5	SA_DQ_54
DDR A D55	AN10	SA_DQ_55
DDR A D56	AM11	SA_DQ_56
DDR A D57	AM5	SA_DQ_57
DDR A D58	AJ9	SA_DQ_58
DDR A D59	AJ8	SA_DQ_59
DDR A D60	AM12	SA_DQ_60
DDR A D61	AM13	SA_DQ_61
DDR A D62	AJ11	SA_DQ_62
DDR A D63	AJ12	SA_DQ_63

CANTIGA_1p0

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0
SA_BS_1	BG18	DDR A BS1
SA_BS_2	AT25	DDR A BS2
SA_RAS#	BB20	DDR A RAS#
SA_CAS#	BD20	DDR A CAS#
SA_WE#	AY20	DDR A WE#
SA_DM_0	AM37	DDR A DM0
SA_DM_1	AT41	DDR A DM1
SA_DM_2	AY41	DDR A DM2
SA_DM_3	AU39	DDR A DM3
SA_DM_4	BB12	DDR A DM4
SA_DM_5	AY6	DDR A DM5
SA_DM_6	AT7	DDR A DM6
SA_DM_7	AJ5	DDR A DM7
SA_DQS_0	AJ44	DDR A DQS0
SA_DQS_1	AT44	DDR A DQS1
SA_DQS_2	BA43	DDR A DQS2
SA_DQS_3	BC37	DDR A DQS3
SA_DQS_4	AW12	DDR A DQS4
SA_DQS_5	BC8	DDR A DQS5
SA_DQS_6	AJ8	DDR A DQS6
SA_DQS_7	AM7	DDR A DQS7
SA_DQS#_0	AJ43	DDR A DQS#0
SA_DQS#_1	AT43	DDR A DQS#1
SA_DQS#_2	BA44	DDR A DQS#2
SA_DQS#_3	BD37	DDR A DQS#3
SA_DQS#_4	AY42	DDR A DQS#4
SA_DQS#_5	BD8	DDR A DQS#5
SA_DQS#_6	AJ9	DDR A DQS#6
SA_DQS#_7	AM8	DDR A DQS#7
SA_MA_0	BA21	DDR A MA0
SA_MA_1	BC24	DDR A MA1
SA_MA_2	BG24	DDR A MA2
SA_MA_3	BH24	DDR A MA3
SA_MA_4	BG25	DDR A MA4
SA_MA_5	BA24	DDR A MA5
SA_MA_6	BD24	DDR A MA6
SA_MA_7	BG27	DDR A MA7
SA_MA_8	BF25	DDR A MA8
SA_MA_9	AW24	DDR A MA9
SA_MA_10	BC21	DDR A MA10
SA_MA_11	BG26	DDR A MA11
SA_MA_12	BH26	DDR A MA12
SA_MA_13	BH17	DDR A MA13
SA_MA_14	AY25	DDR A MA14

[15] DDR_B_D[0..63]

DDR B D0	AK47	SB_DQ_0
DDR B D1	AH46	SB_DQ_1
DDR B D2	AP47	SB_DQ_2
DDR B D3	AP46	SB_DQ_3
DDR B D4	AJ46	SB_DQ_4
DDR B D5	AJ48	SB_DQ_5
DDR B D6	AM48	SB_DQ_6
DDR B D7	AP48	SB_DQ_7
DDR B D8	AJ47	SB_DQ_8
DDR B D9	AJ46	SB_DQ_9
DDR B D10	BA48	SB_DQ_10
DDR B D11	AY48	SB_DQ_11
DDR B D12	AT47	SB_DQ_12
DDR B D13	AR47	SB_DQ_13
DDR B D14	BA47	SB_DQ_14
DDR B D15	BC47	SB_DQ_15
DDR B D16	BC46	SB_DQ_16
DDR B D17	BC44	SB_DQ_17
DDR B D18	BG43	SB_DQ_18
DDR B D19	BF43	SB_DQ_19
DDR B D20	BE45	SB_DQ_20
DDR B D21	BC41	SB_DQ_21
DDR B D22	BE40	SB_DQ_22
DDR B D23	BE41	SB_DQ_23
DDR B D24	BG38	SB_DQ_24
DDR B D25	BF38	SB_DQ_25
DDR B D26	BH35	SB_DQ_26
DDR B D27	BG35	SB_DQ_27
DDR B D28	BH40	SB_DQ_28
DDR B D29	BG39	SB_DQ_29
DDR B D30	BG34	SB_DQ_30
DDR B D31	BH34	SB_DQ_31
DDR B D32	BH14	SB_DQ_32
DDR B D33	BG12	SB_DQ_33
DDR B D34	BH11	SB_DQ_34
DDR B D35	BG8	SB_DQ_35
DDR B D36	BH12	SB_DQ_36
DDR B D37	BE11	SB_DQ_37
DDR B D38	BF8	SB_DQ_38
DDR B D39	BG7	SB_DQ_39
DDR B D40	BC5	SB_DQ_40
DDR B D41	BC6	SB_DQ_41
DDR B D42	AY3	SB_DQ_42
DDR B D43	AY1	SB_DQ_43
DDR B D44	BE6	SB_DQ_44
DDR B D45	BF5	SB_DQ_45
DDR B D46	BA1	SB_DQ_46
DDR B D47	BD3	SB_DQ_47
DDR B D48	AV2	SB_DQ_48
DDR B D49	AJ3	SB_DQ_49
DDR B D50	AR3	SB_DQ_50
DDR B D51	AN2	SB_DQ_51
DDR B D52	AY2	SB_DQ_52
DDR B D53	AV1	SB_DQ_53
DDR B D54	AP3	SB_DQ_54
DDR B D55	AR1	SB_DQ_55
DDR B D56	AL1	SB_DQ_56
DDR B D57	AL2	SB_DQ_57
DDR B D58	AJ1	SB_DQ_58
DDR B D59	AM2	SB_DQ_59
DDR B D60	AM1	SB_DQ_60
DDR B D61	AM3	SB_DQ_61
DDR B D62	AH3	SB_DQ_62
DDR B D63	AJ3	SB_DQ_63

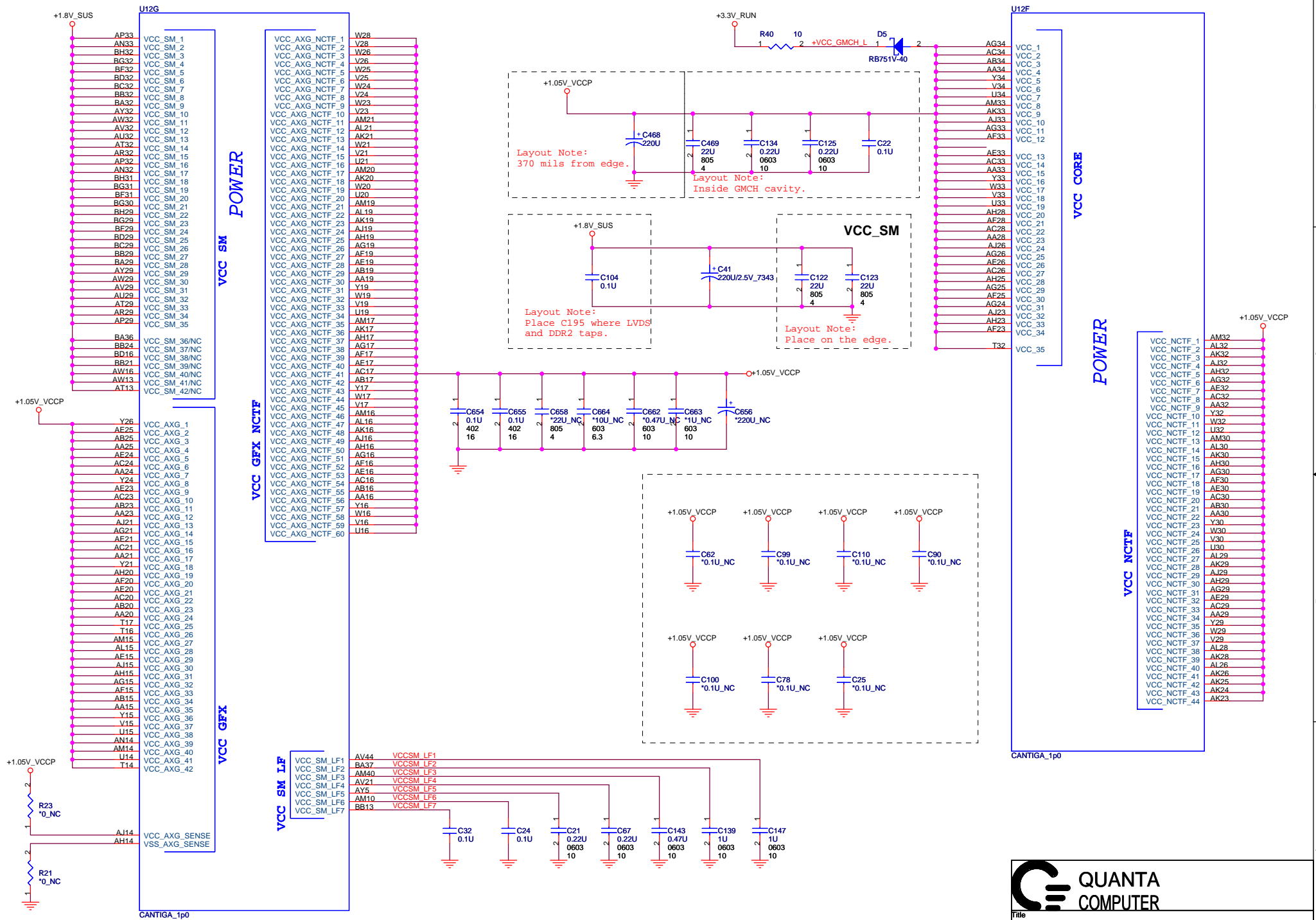
CANTIGA_1p0

DDR SYSTEM MEMORY B


SB_BS_0	BC16	DDR B BS0
SB_BS_1	BB17	DDR B BS1
SB_BS_2	BB33	DDR B BS2
SB_RAS#	AJ17	DDR B RAS#
SB_CAS#	BG16	DDR B CAS#
SB_WE#	BF14	DDR B WE#
SB_DM_0	AM47	DDR B DM0
SB_DM_1	AY47	DDR B DM1
SB_DM_2	BD40	DDR B DM2
SB_DM_3	BF35	DDR B DM3
SB_DM_4	BG11	DDR B DM4
SB_DM_5	BA3	DDR B DM5
SB_DM_6	AP1	DDR B DM6
SB_DM_7	AK2	DDR B DM7
SB_DQS_0	AL47	DDR B DQS0
SB_DQS_1	AV48	DDR B DQS1
SB_DQS_2	BG41	DDR B DQS2
SB_DQS_3	BG37	DDR B DQS3
SB_DQS_4	BH9	DDR B DQS4
SB_DQS_5	BB2	DDR B DQS5
SB_DQS_6	AJ1	DDR B DQS6
SB_DQS_7	AN6	DDR B DQS7
SB_DQS#_0	AL46	DDR B DQS#0
SB_DQS#_1	AV47	DDR B DQS#1
SB_DQS#_2	BH41	DDR B DQS#2
SB_DQS#_3	BH37	DDR B DQS#3
SB_DQS#_4	BC2	DDR B DQS#4
SB_DQS#_5	AT2	DDR B DQS#5
SB_DQS#_6	AN5	DDR B DQS#6
SB_DQS#_7	AN5	DDR B DQS#7
SB_MA_0	AV17	DDR B MA0
SB_MA_1	BA25	DDR B MA1
SB_MA_2	BC25	DDR B MA2
SB_MA_3	AU25	DDR B MA3
SB_MA_4	AW25	DDR B MA4
SB_MA_5	BB28	DDR B MA5
SB_MA_6	AU28	DDR B MA6
SB_MA_7	AW28	DDR B MA7
SB_MA_8	AT33	DDR B MA8
SB_MA_9	BD33	DDR B MA9
SB_MA_10	BB16	DDR B MA10
SB_MA_11	AW33	DDR B MA11
SB_MA_12	AY33	DDR B MA12
SB_MA_13	BH15	DDR B MA13
SB_MA_14	AU33	DDR B MA14



Title			
Cantiga (DDR2)			
Size	Document Number		Rev
	VM8G		1B
Date:	Saturday, June 06, 2009	Sheet 7 of 53	

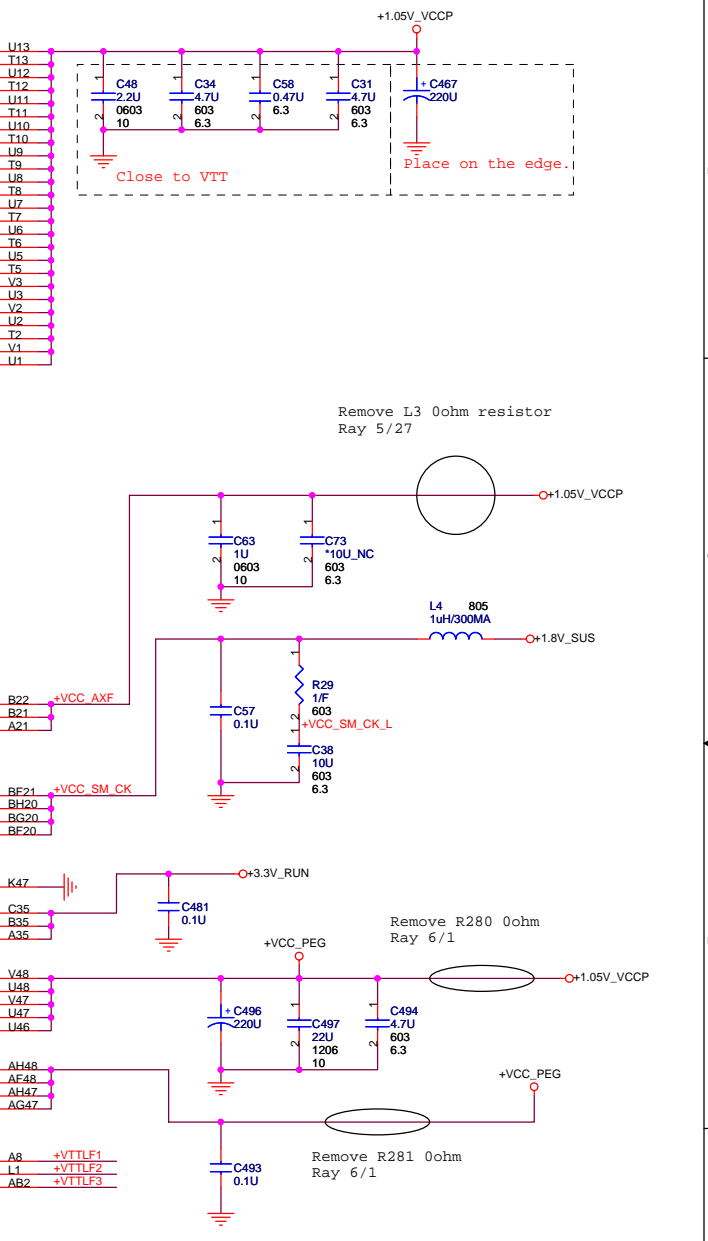
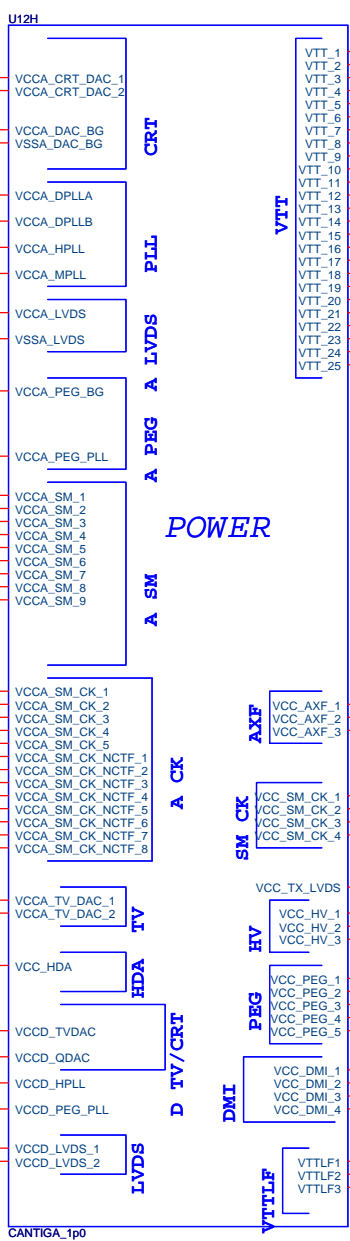
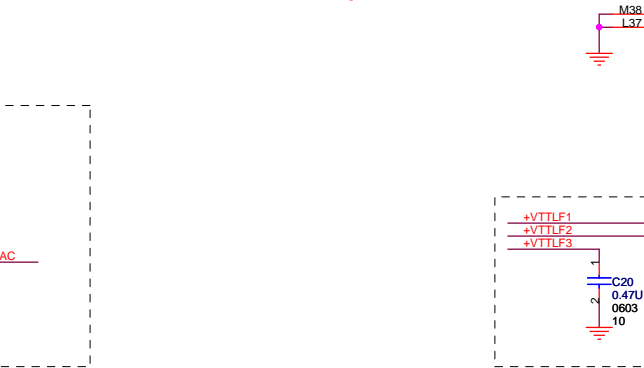
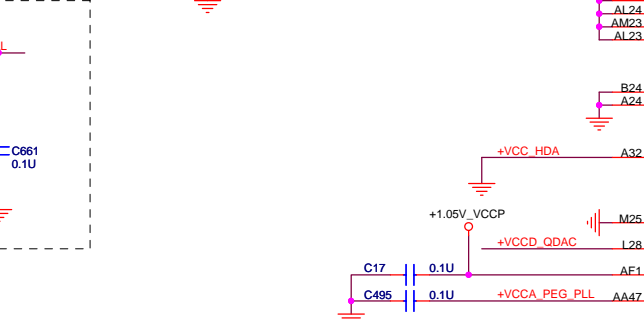
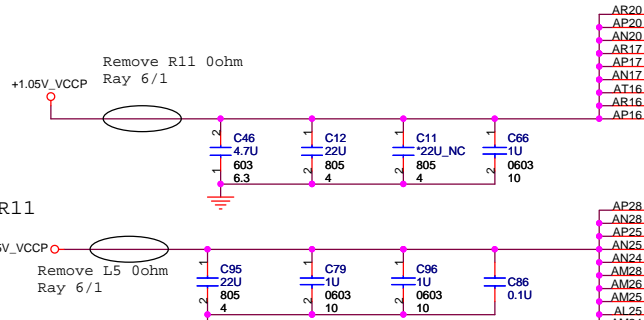
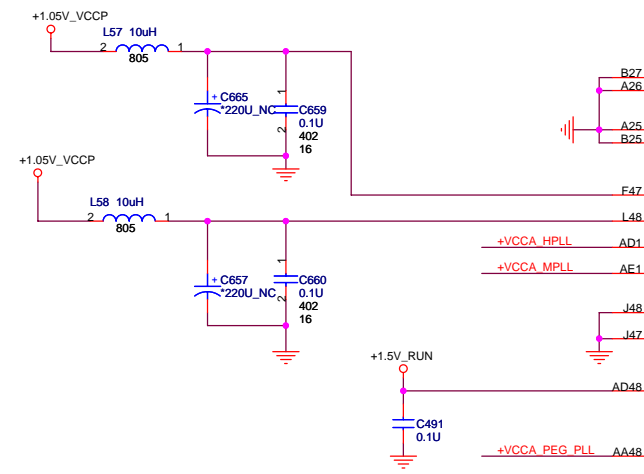
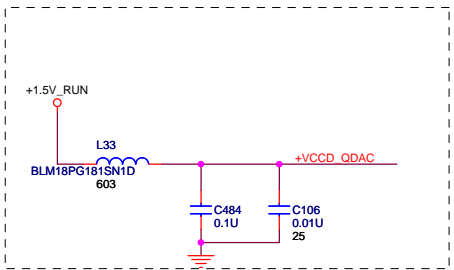
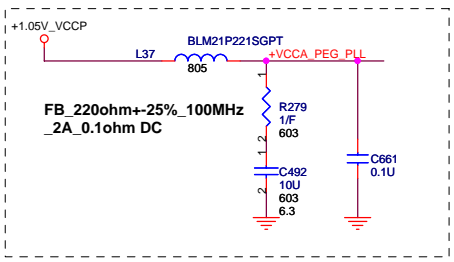
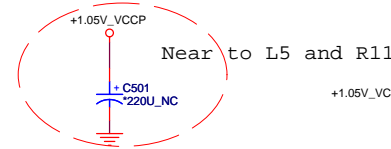
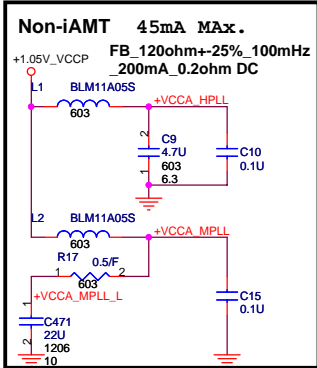


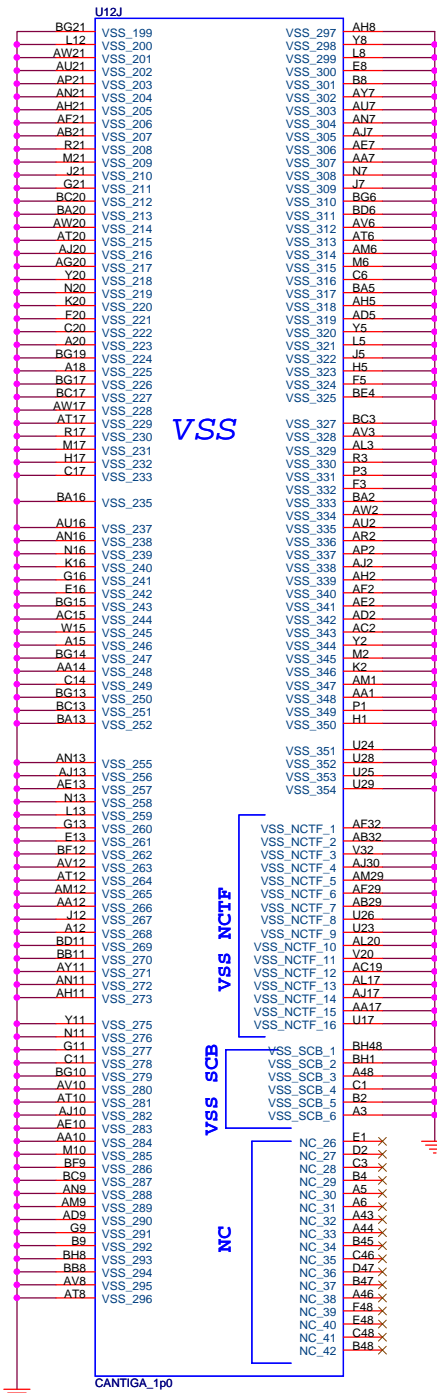
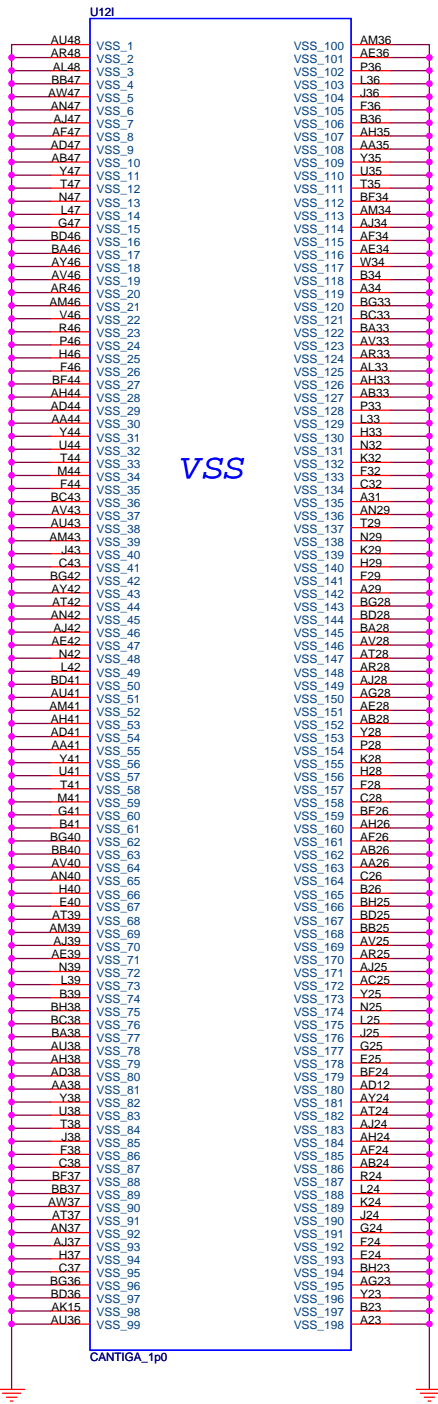
UMA: Places R21, R23 to 10 ohm.
Dis: Please R21, R23 to 0 ohm.




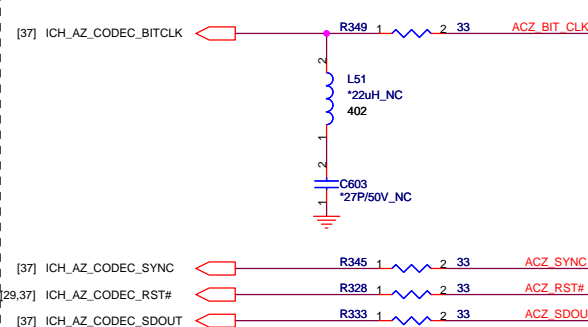
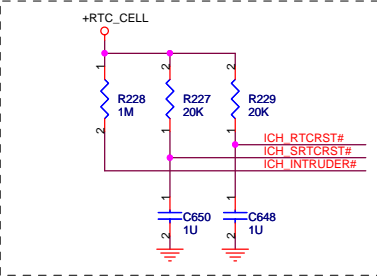
QUANTA
COMPUTER

Title Cantiga (VCC,NCTF)		
Size VM8G	Document Number	Rev 1B
Date: Saturday, June 06, 2009	Sheet 8	of 53

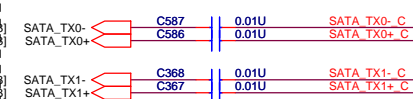




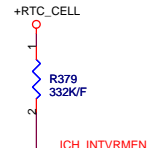
		QUANTA COMPUTER	
File: Cantiga (VSS)			
Size: VM8G	Document Number		Rev 1B
Date: Saturday, June 06, 2009	Sheet 10	of 53	



Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.

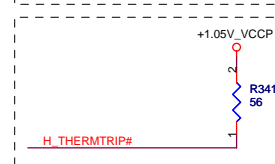
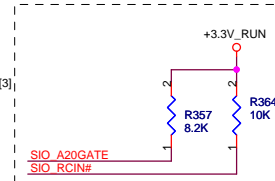
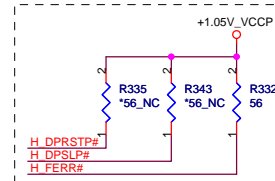
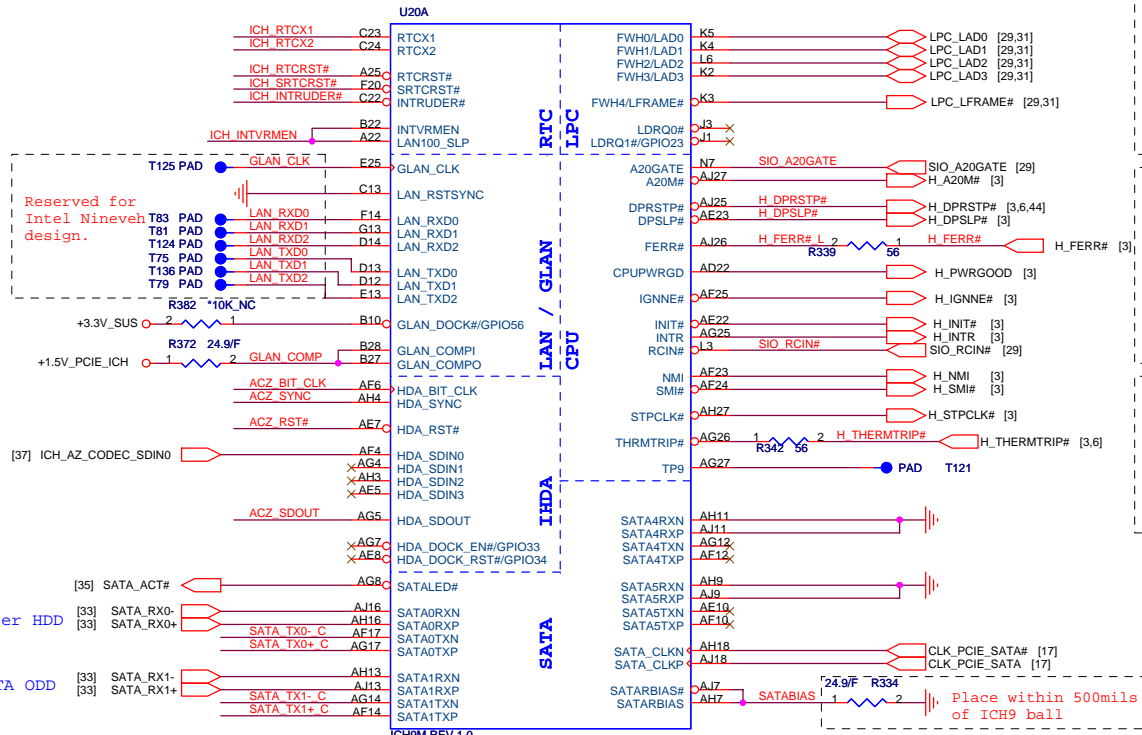


SATA TX/RX capacitor need near to the connector



ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



ICH_RSVD	ACZ_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1

The diagram also shows a circuit connection for the ACZ_SDOUT signal. It is connected to a node between two resistors, R340 (1K_NC) and R387 (1K_NC), which are connected to a +3.3V_RUN supply and ground. This node is also labeled ICH_RSVD [13].



QUANTA
COMPUTER

Title	ICH9-M (CPU,SATA,LPC,LAN,CODEC)
-------	---------------------------------

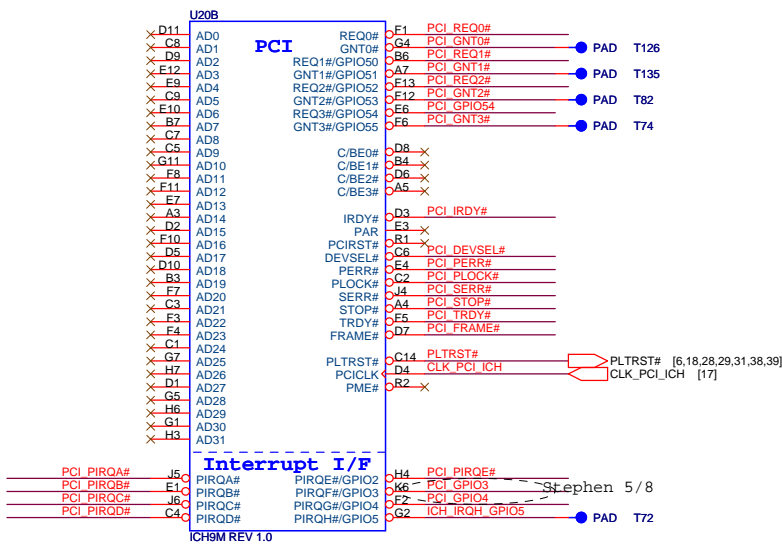
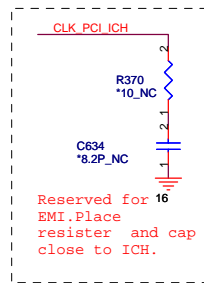
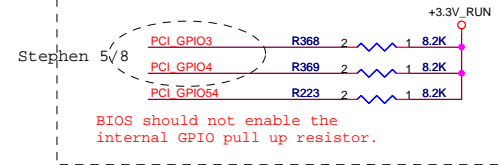
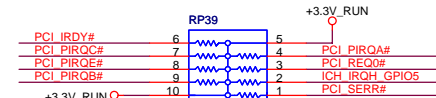
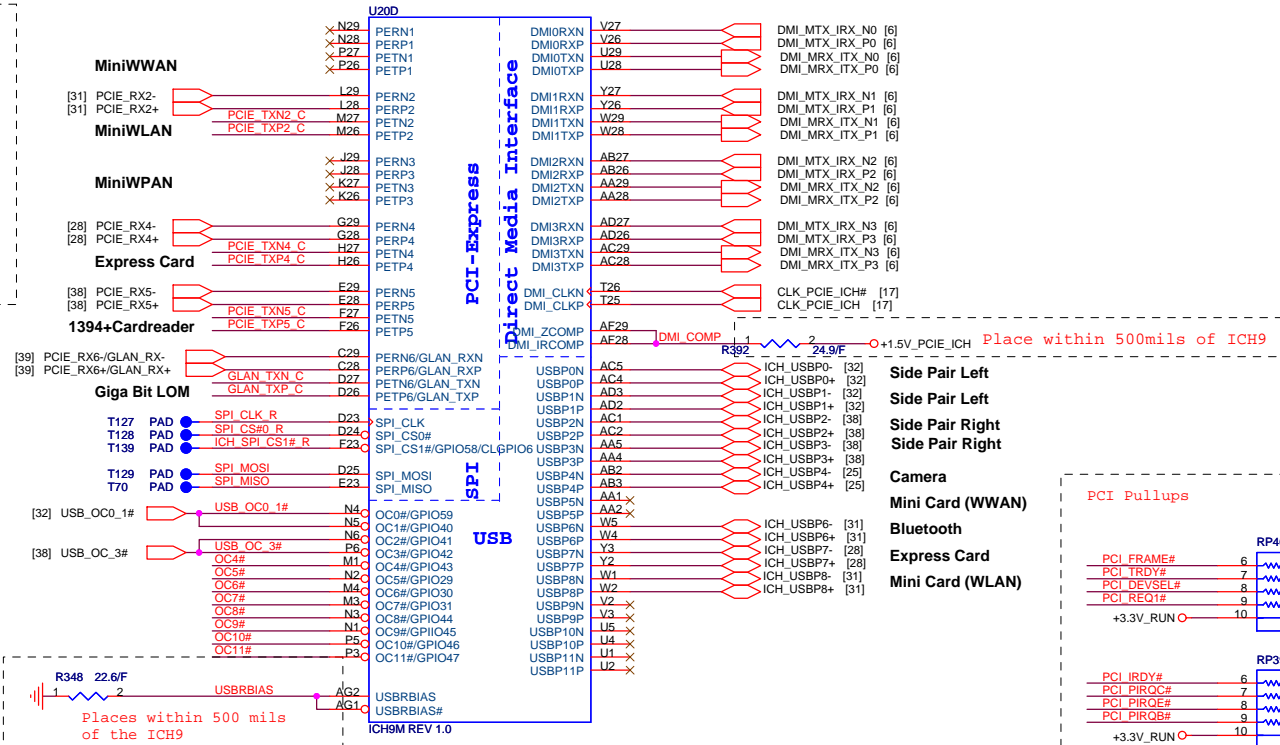
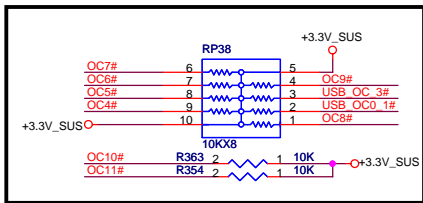
Size	Document Number VM8G
------	-------------------------

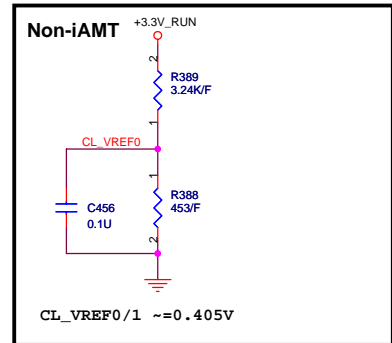
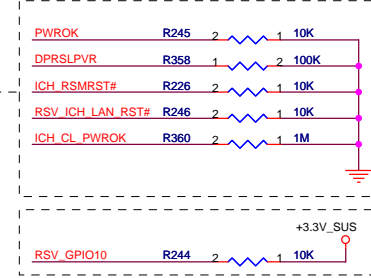
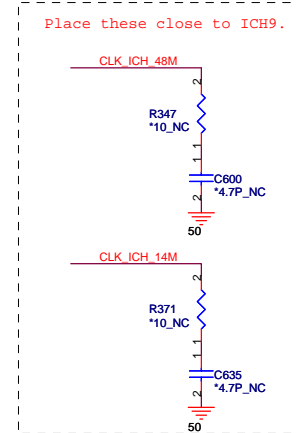
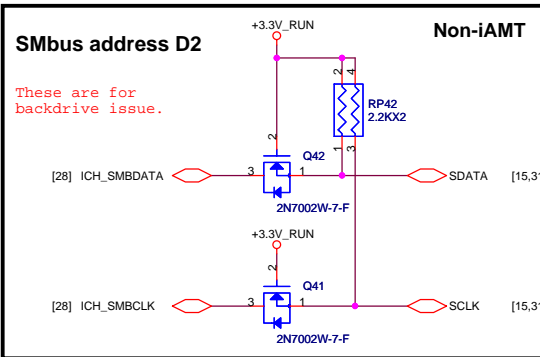
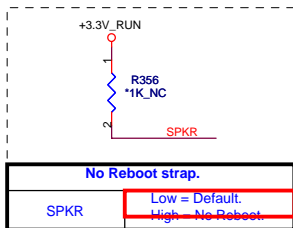
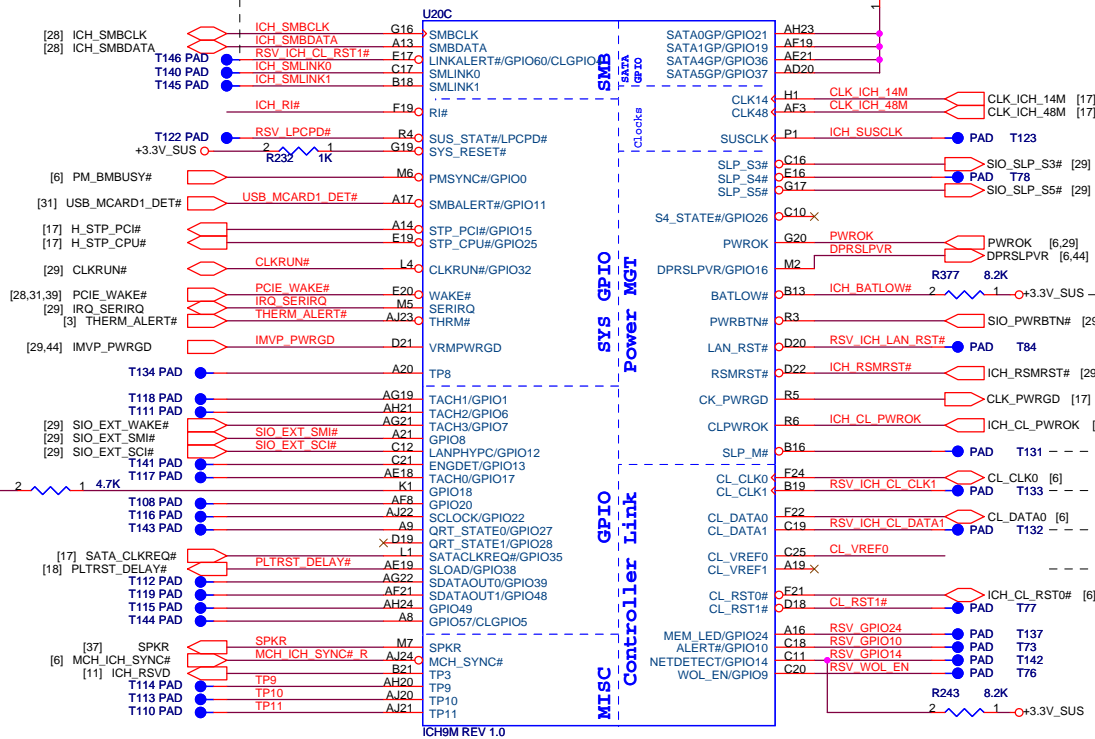
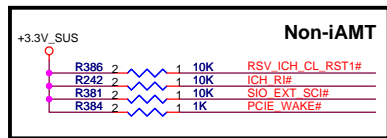
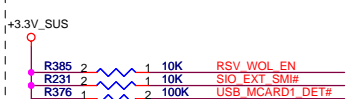
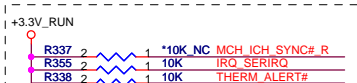
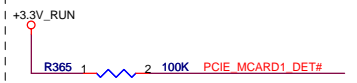
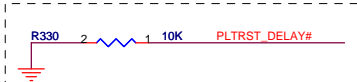
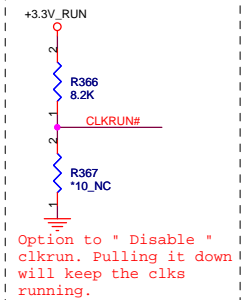
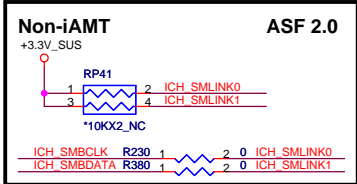
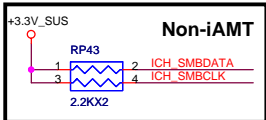
Date: Saturday, June 06, 2009 Sheet 11 of 53

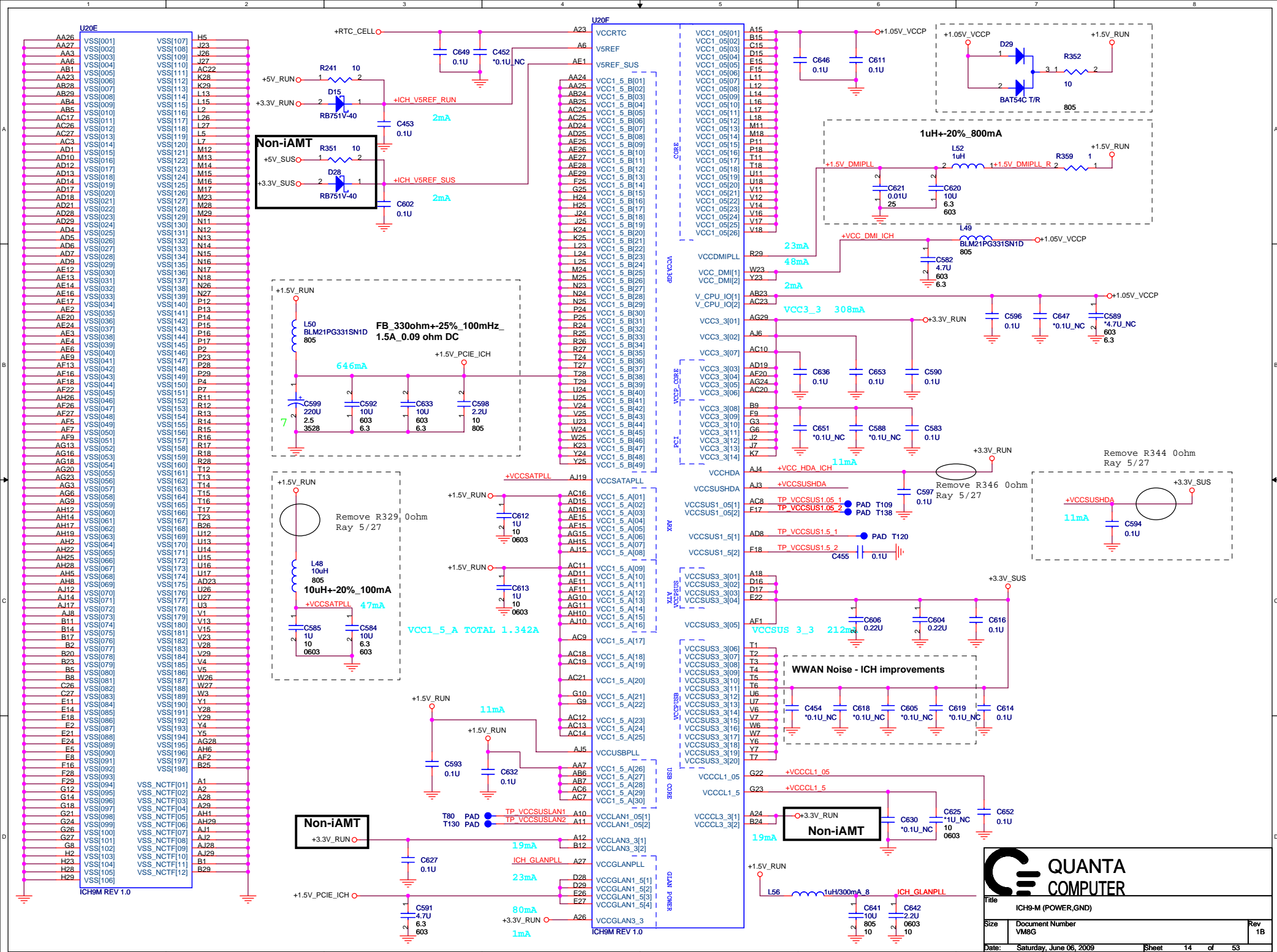
Date: Saturday, June 06, 2009 Sheet 11 of 53

Date: Saturday, June 06, 2009 Sheet 11 of 53

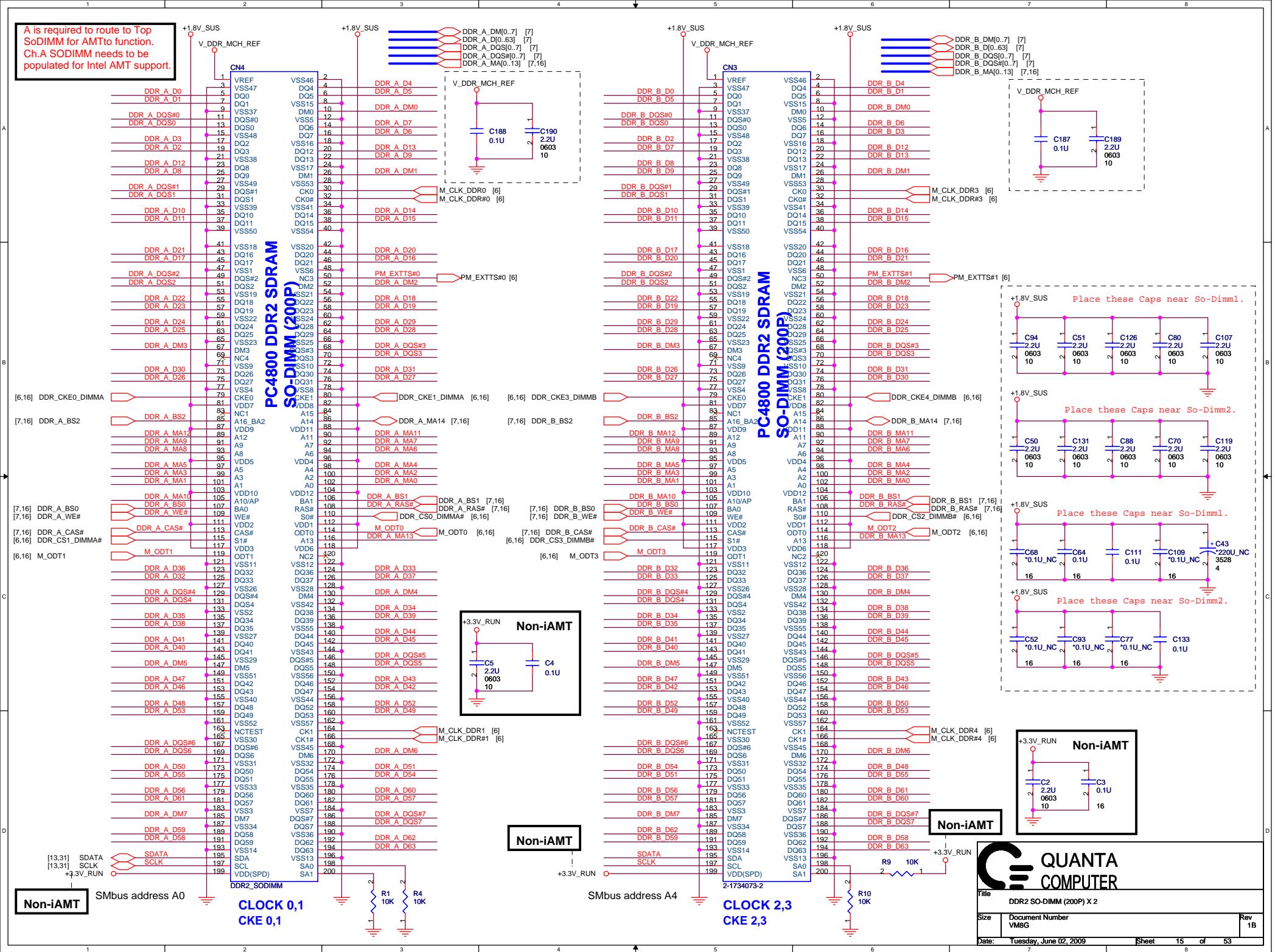
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

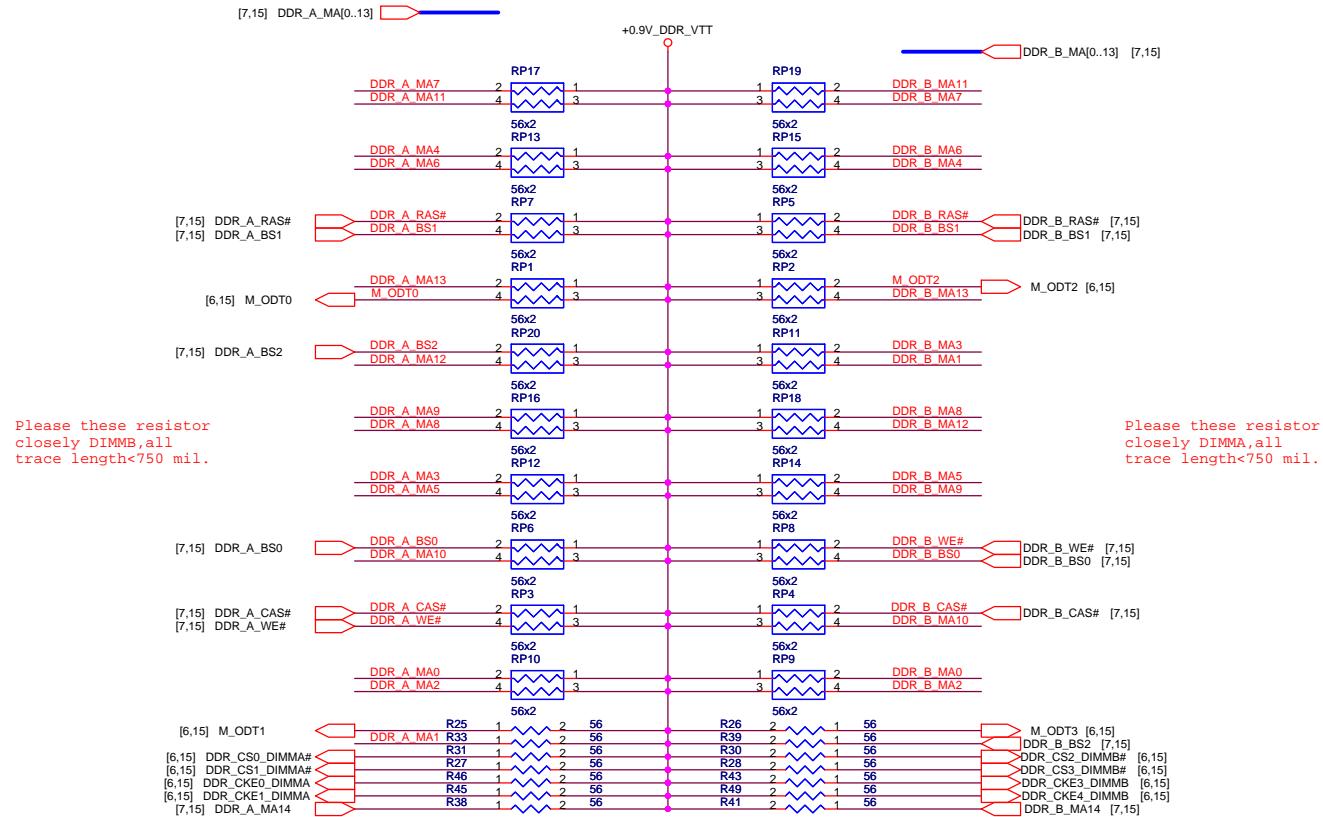
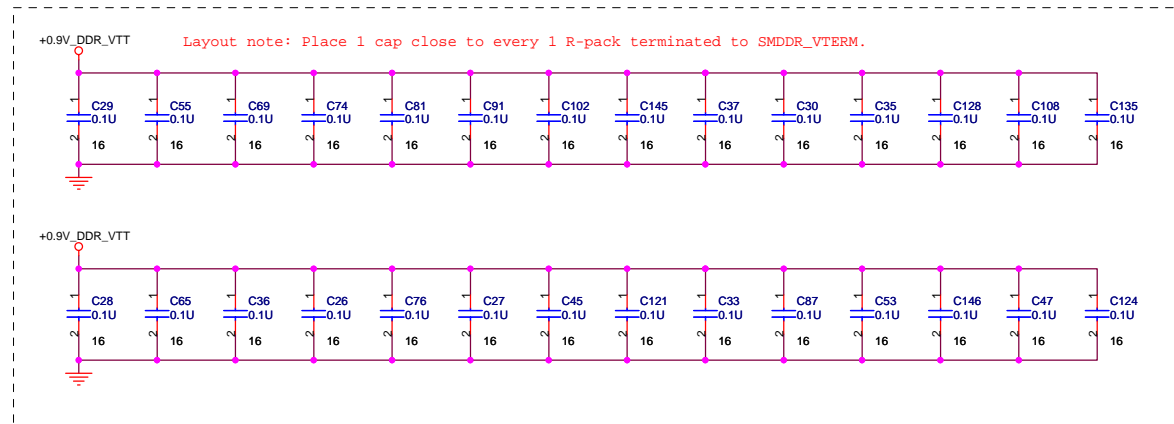




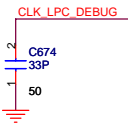
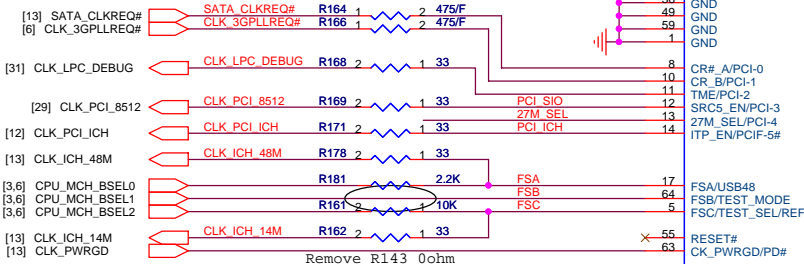
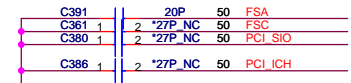


A is required to route to Top SoDIMM for AMTto function.
Ch.A SODIMM needs to be populated for Intel AMT support.



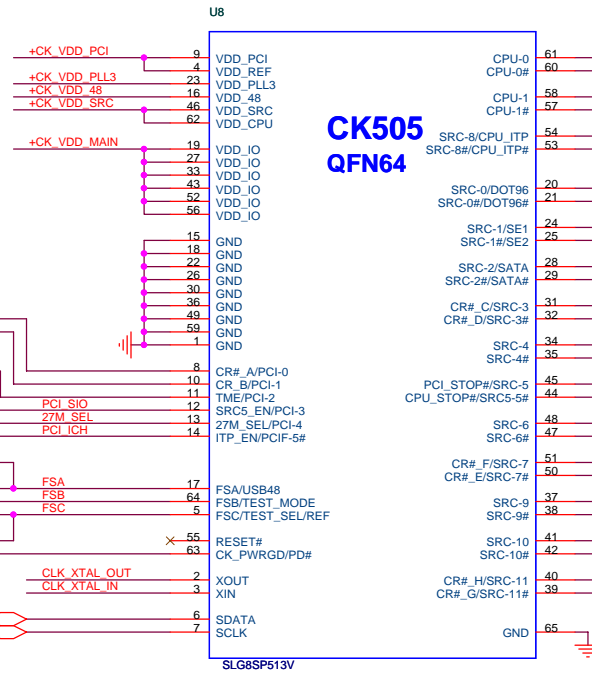


Add capacitor pads for improving WWAN.

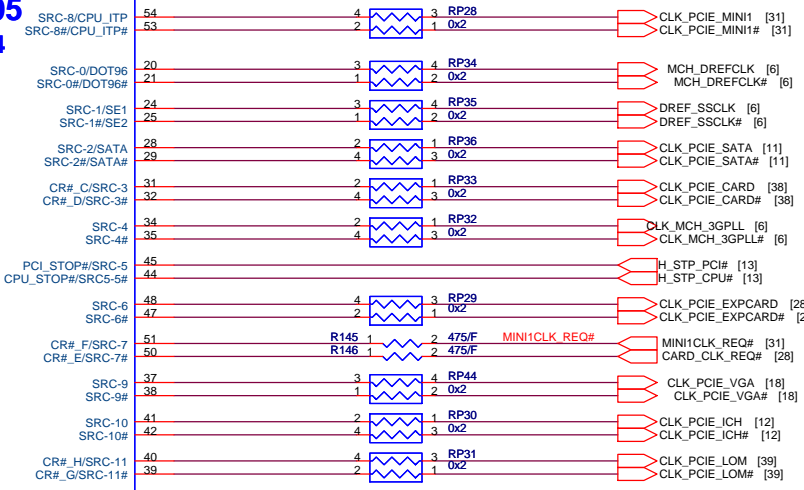


Remove R143 0ohm
Ray 5/27

[3,25,29] SMBDAT1
[3,25,29] SMBCLK1



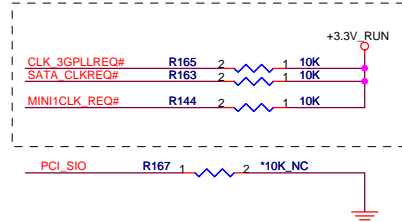
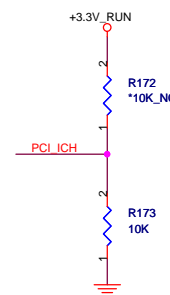
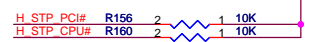
CK505
QFN64



Express Card

ITP_EN

PCI_ICH	10K-pull
0	Disable
1	Enable



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



[6] PCIE_MTX_GRX_P[0..15]
[6] PCIE_MTX_GRX_N[0..15]

PCIE_MTX_GRX_P0 AF30
PCIE_MTX_GRX_N0 AE31

PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28

PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31

PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28

PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31

PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28

PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31

PCIE_MTX_GRX_P7 W29
PCIE_MTX_GRX_N7 V28

PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31

PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28

PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31

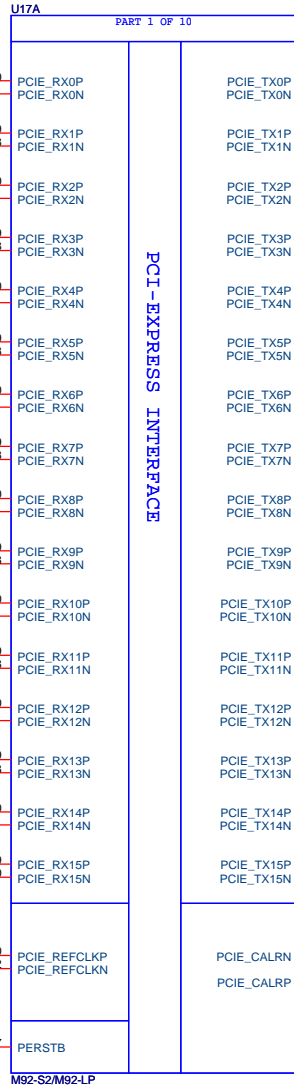
PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28

PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31

PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28

PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31

PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30



PCIE_TX0P AH30
PCIE_TX0N AG31

PCIE_TX1P AG29
PCIE_TX1N AF28

PCIE_TX2P AF27
PCIE_TX2N AF26

PCIE_TX3P AD27
PCIE_TX3N AD26

PCIE_TX4P AC25
PCIE_TX4N AD25

PCIE_TX5P Y23
PCIE_TX5N Y24

PCIE_TX6P AB27
PCIE_TX6N AB26

PCIE_TX7P Y27
PCIE_TX7N Y26

PCIE_TX8P W24
PCIE_TX8N W23

PCIE_TX9P V27
PCIE_TX9N U26

PCIE_TX10P U24
PCIE_TX10N U23

PCIE_TX11P T26
PCIE_TX11N T27

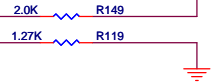
PCIE_TX12P T24
PCIE_TX12N T23

PCIE_TX13P P27
PCIE_TX13N P26

PCIE_TX14P P24
PCIE_TX14N P23

PCIE_TX15P M27
PCIE_TX15N N26

PCIE_CALRN AA22
PCIE_CALRP Y22

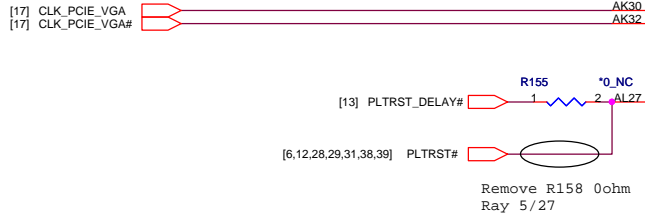


[6] PCIE_MRX_GTX_P[0..15]
[6] PCIE_MRX_GTX_N[0..15]

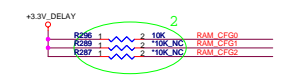
PCIE_MRX_GTX_P0 0.1U 2 1 C350 16 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C345 16 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C342 16 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C347 16 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C349 16 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C376 16 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C357 16 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C373 16 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C355 16 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C353 16 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C340 16 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C372 16 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C338 16 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C370 16 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C364 16 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C560 16 PCIE_MRX_GTX_C_P15

PCIE_MRX_GTX_N0 0.1U 2 1 C351 16 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C344 16 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C343 16 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C346 16 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C348 16 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C375 16 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C356 16 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C374 16 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C354 16 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C352 16 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C339 16 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C371 16 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C337 16 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C369 16 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C363 16 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C561 16 PCIE_MRX_GTX_C_N15

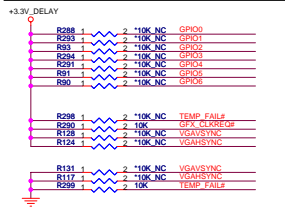
100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
clock must be provided less than 400ns
after CLKREQ# is asserted



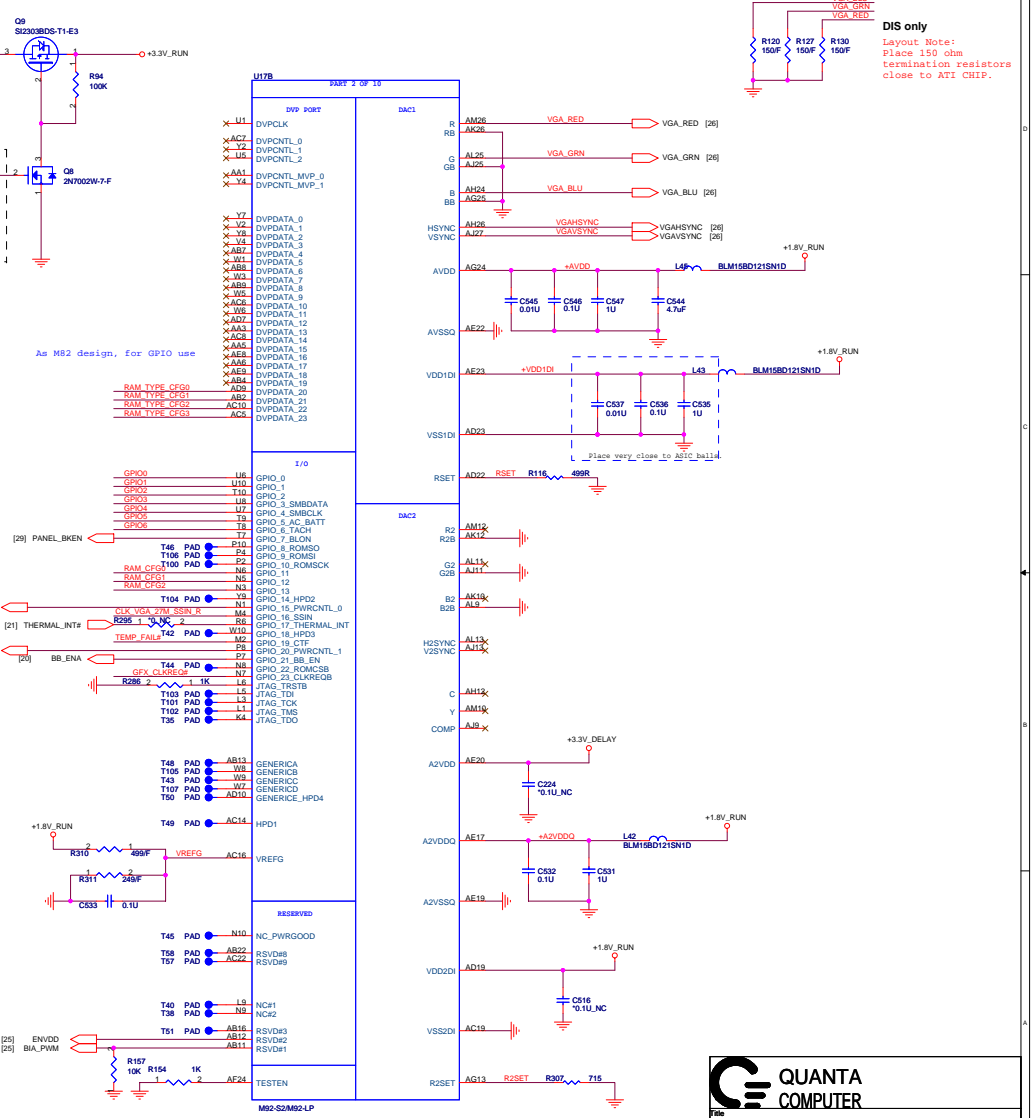
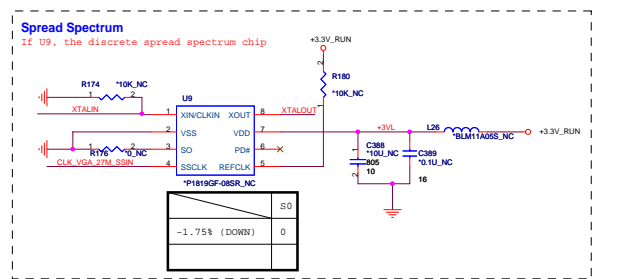
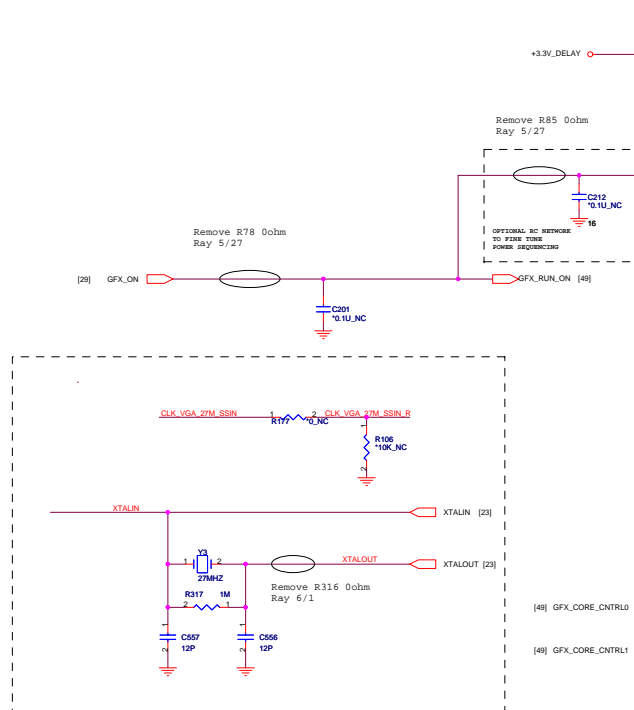
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG1 GP109	CFG2 GP1013	CFG3 GP1012	CFG4 GP1011
128MB	0	0	0	0
256MB	0	0	0	1
64MB	0	0	1	0
512MB	1	0	0	0



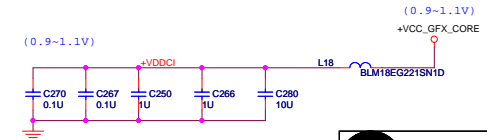
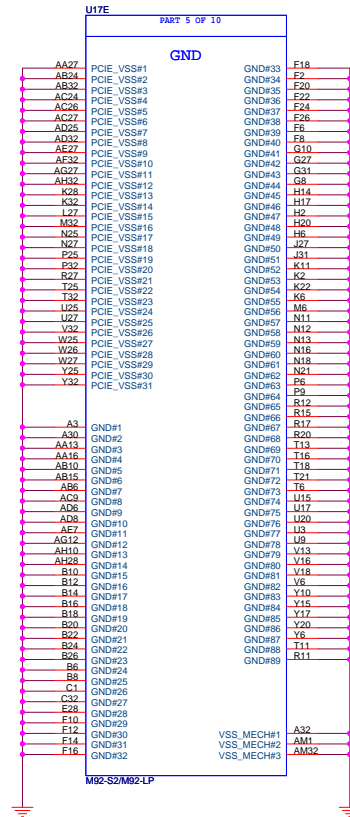
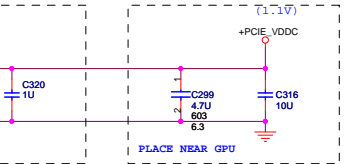
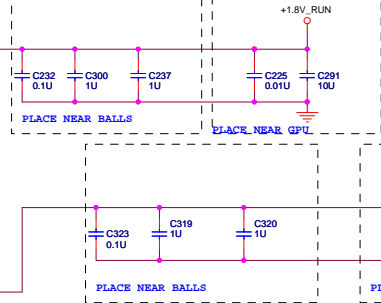
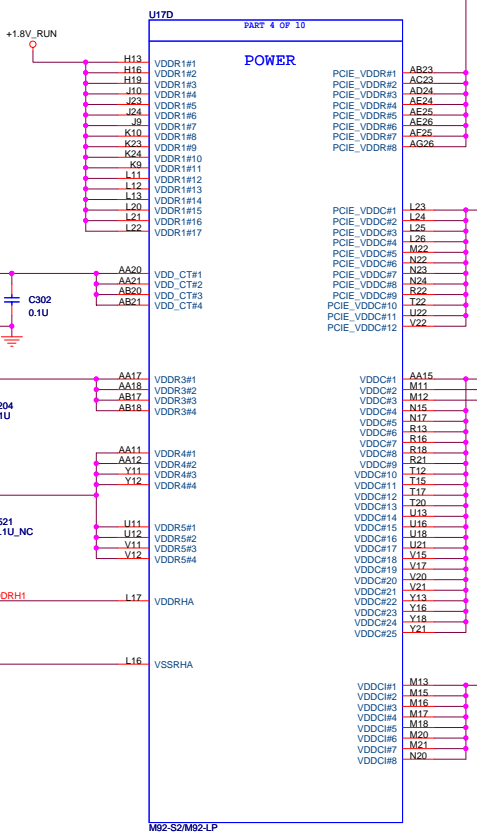
GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	FW setting
GPIO0	GPIO0 - TX_PWR5_EN (Transmitter Power Savings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - TX_DEEMPH_EN (Transmitter De-emphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - RIF_GEN0_EN (5.6 GTx Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO 5, AC, BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI Internal use only	0



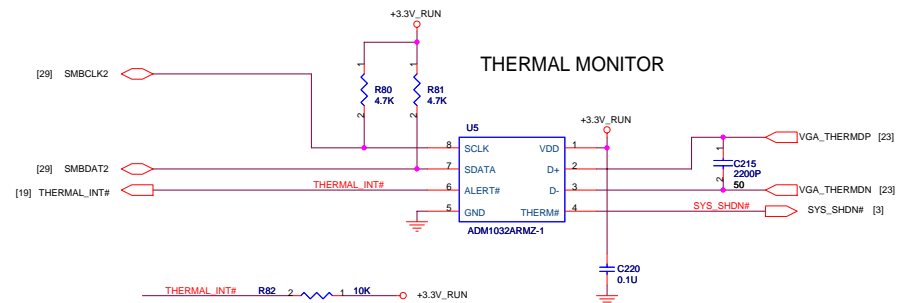
Memory Straps	RAM_TYPE	BEAM_TYPE	CFG1	CFG2	CFG3	CFG4	Quantia PN (QuantaBuy)	Vendor PN
500MHz 512MB(64M*16) Hynix	0	0	1	0			AKD5LG-TW01(FR)	H5PS1G63KFR-20L
Remove Qionda Source								
500MHz 512MB(64M*16) Samsung	0	0	0	1			AKD5LG-T507(IE)	K4N1G164QE-HC20
Remove								



The diagram illustrates a decoupling network for a GPU. A +1.8V RUN supply is connected to a series of capacitors: C227 (100), C228 (100uF), C239 (1u), C231 (1u), and C253 (0.1u). The capacitors are connected in parallel to ground. Labels indicate 'PLACE NEAR GPU' for C227 and C228, and 'PLACE NEAR BALLS' for C239, C231, and C253.

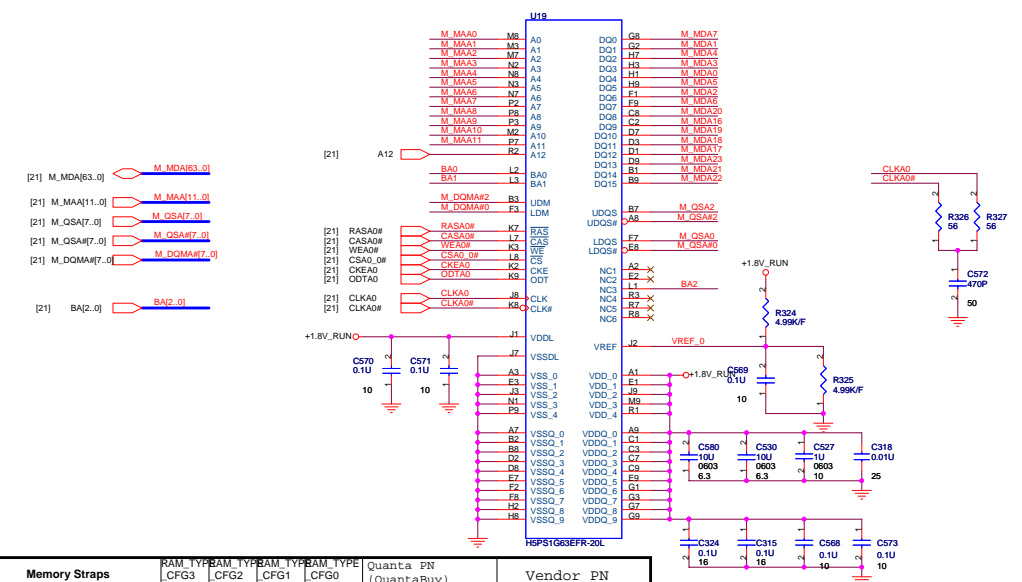


MEMORY INTERFACE

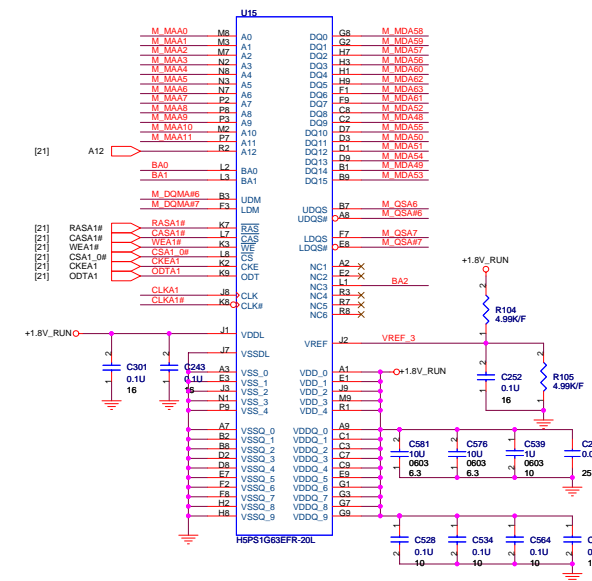
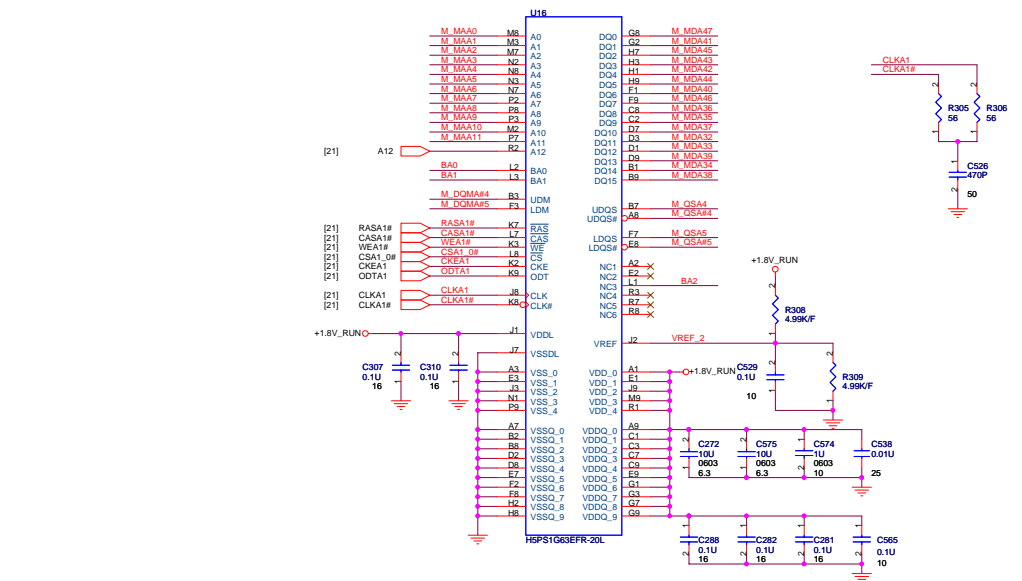
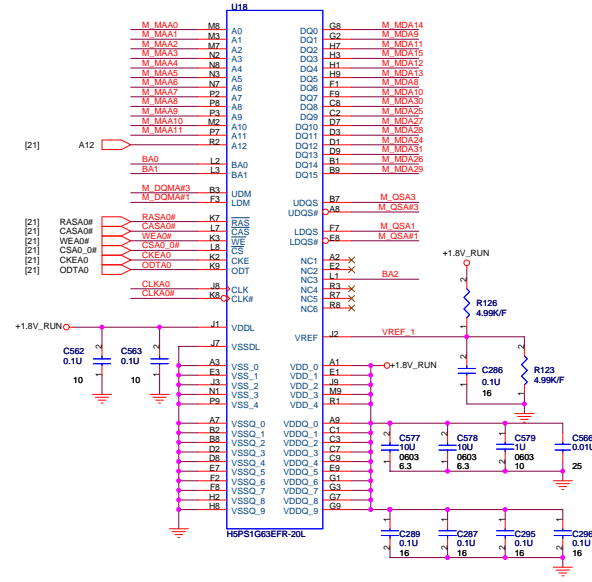


DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

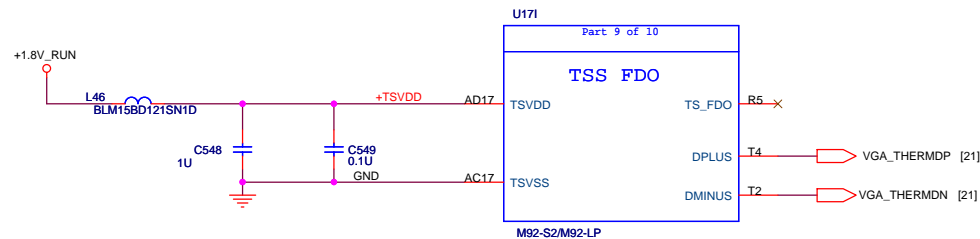
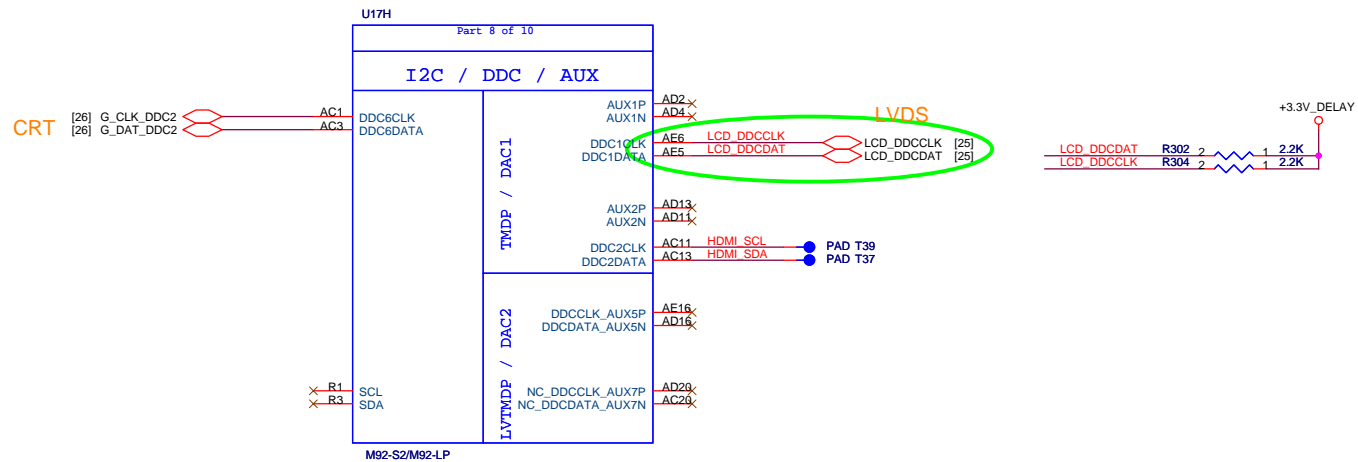
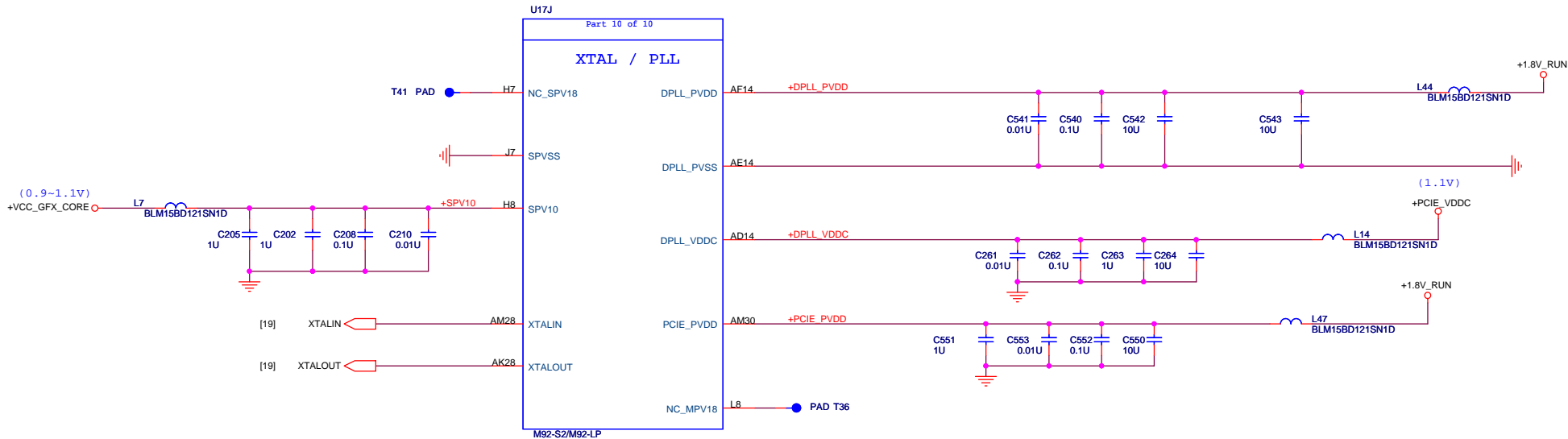
DDR2 64MbitX16 MEMORY



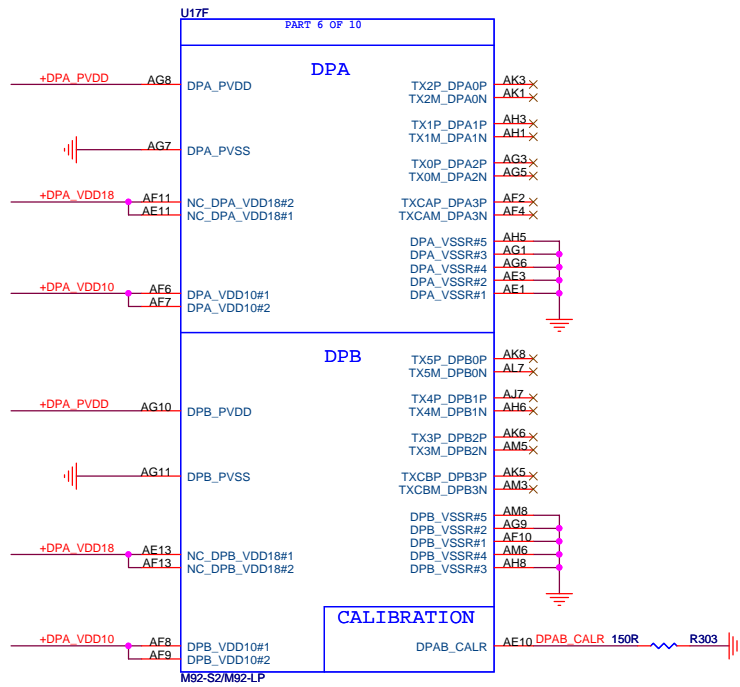
Memory Straps	RAM TYPE	RAM TYPE	RAM TYPE	RAM TYPE	Quanta PN (QuantaBuy)	Vendor PN
	CFG3	CFG2	CFG1	CFG0		
500MHz 512MB(64M*16) Hynix	0	0	1	0	AKD5LG-TW01 (FR)	H5PS1G63EFR-20L
Remove Qimonda						
500MHz 512MB(64M*16) Samsung	0	0	0	1	AKD5LG-T507 (IE)	K4N1G164QE-HC20
Remove						



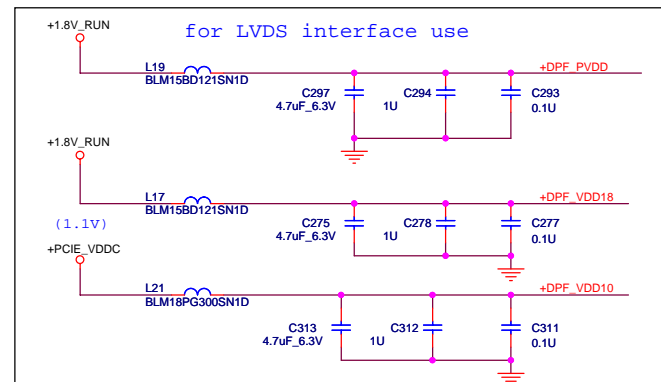
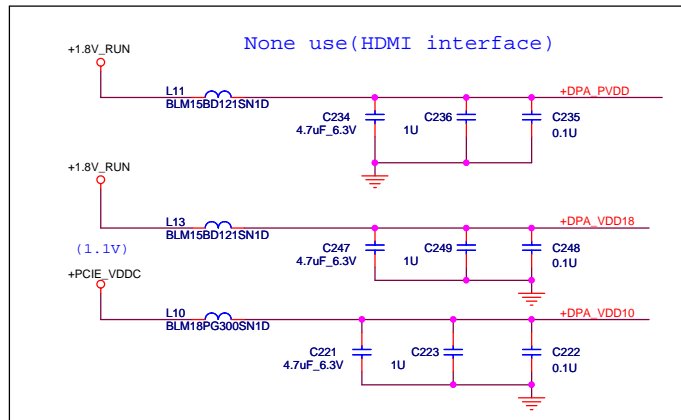
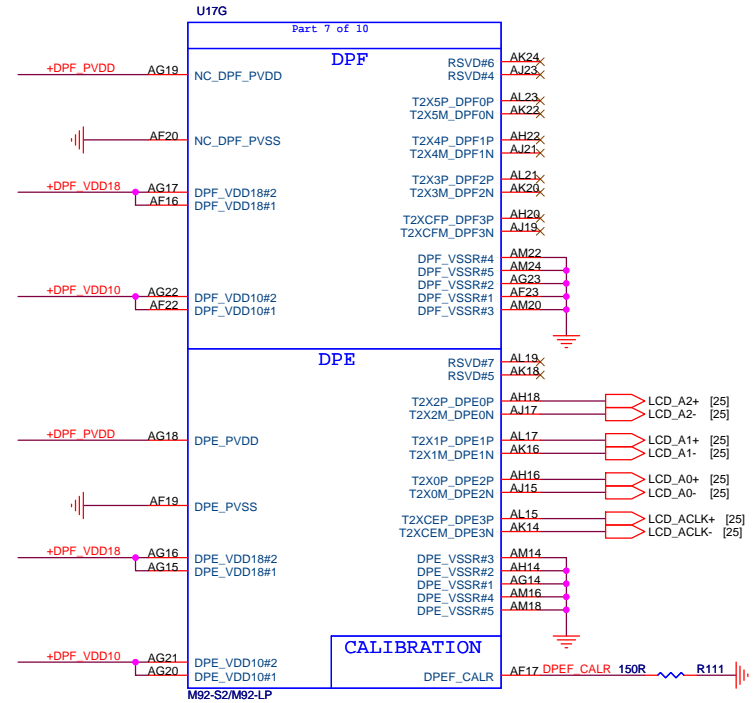
Title		
M92-S2_DDR2_512M		
Size	Document Number	Rev
	VM8G	1B
Date:	Saturday, June 06, 2009	Sheet 22 of 53



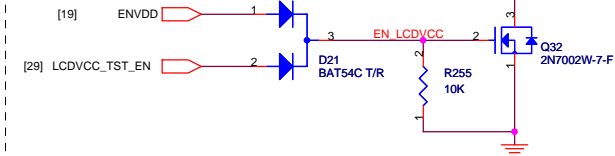
TMDP(HDMI) INTERFACE



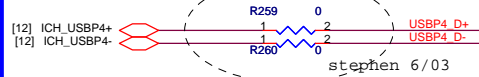
LVDS INTERFACE



Support the new imbedded diagnostics.

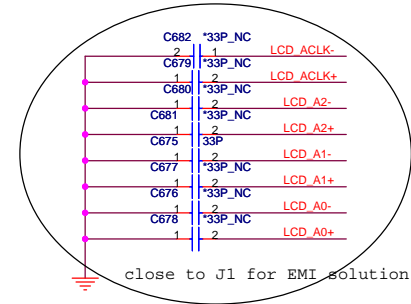
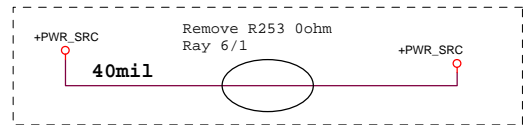
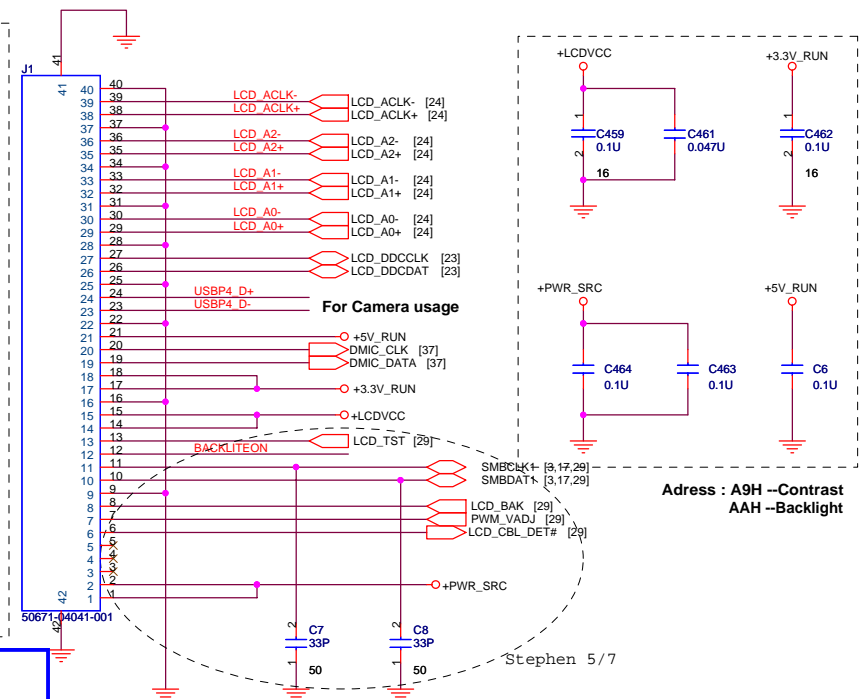
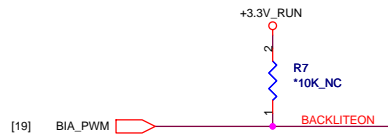


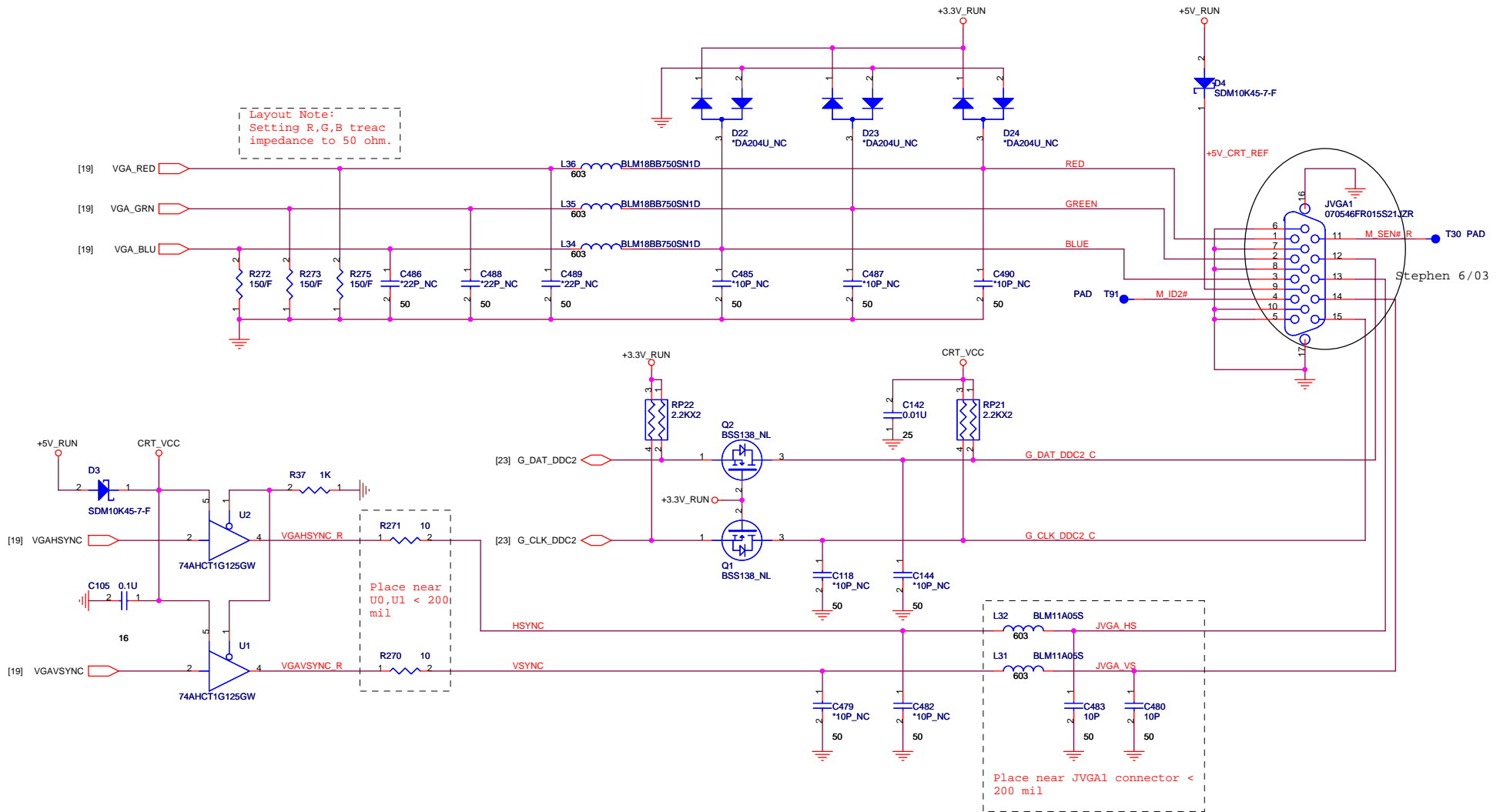
Camera support




stephen 6/03

For DPST support





	A	B	C	D	E
1					
2					
3					
4					



QUANTA

COMPUTER

Title

Card Reader-RTS5158E

Size

Document Number

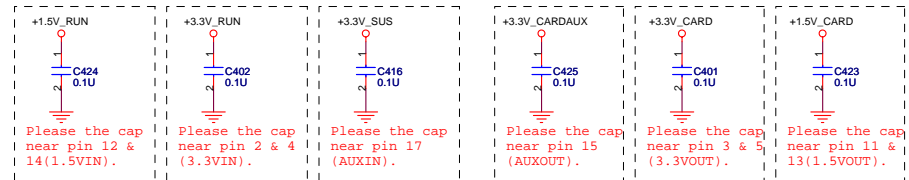
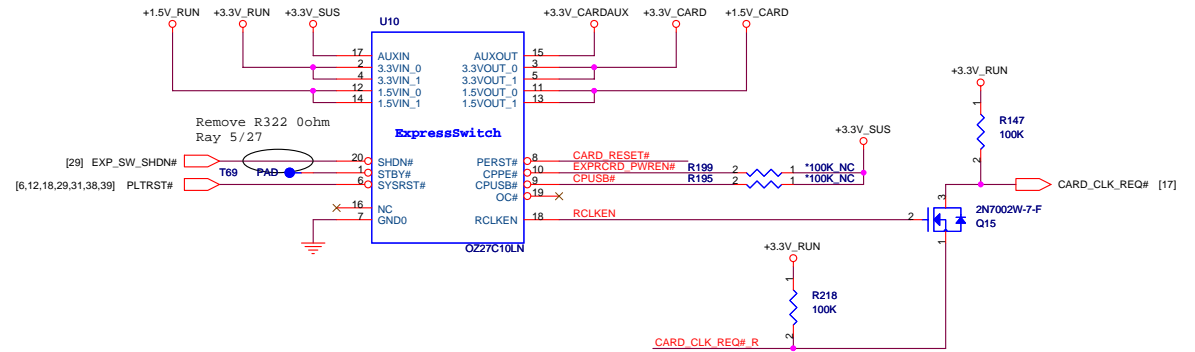
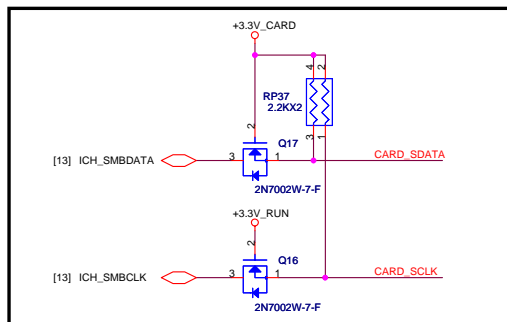
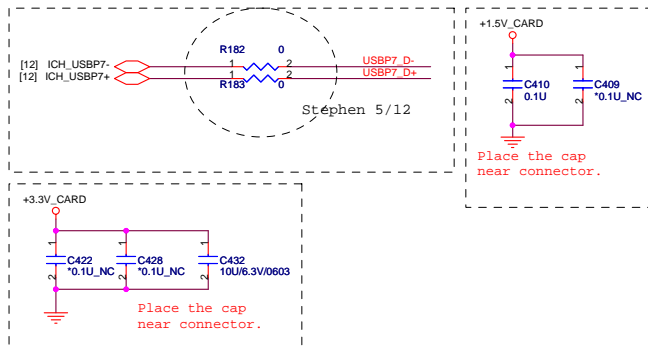
Rev

VM8G

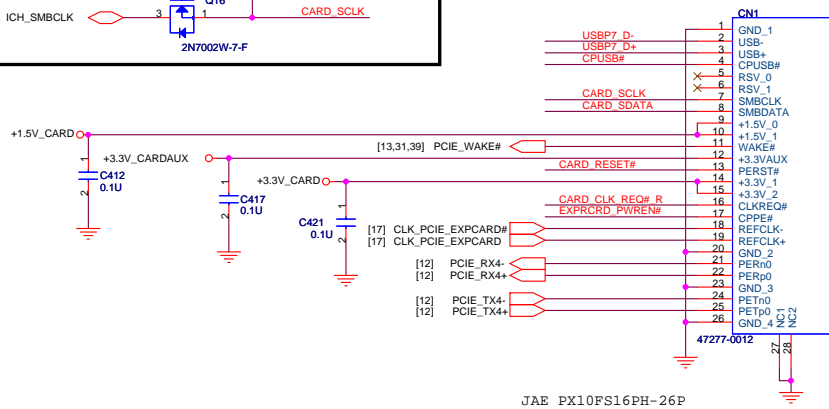
1B

Date: Tuesday, June 02, 2009

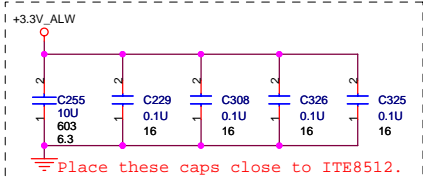
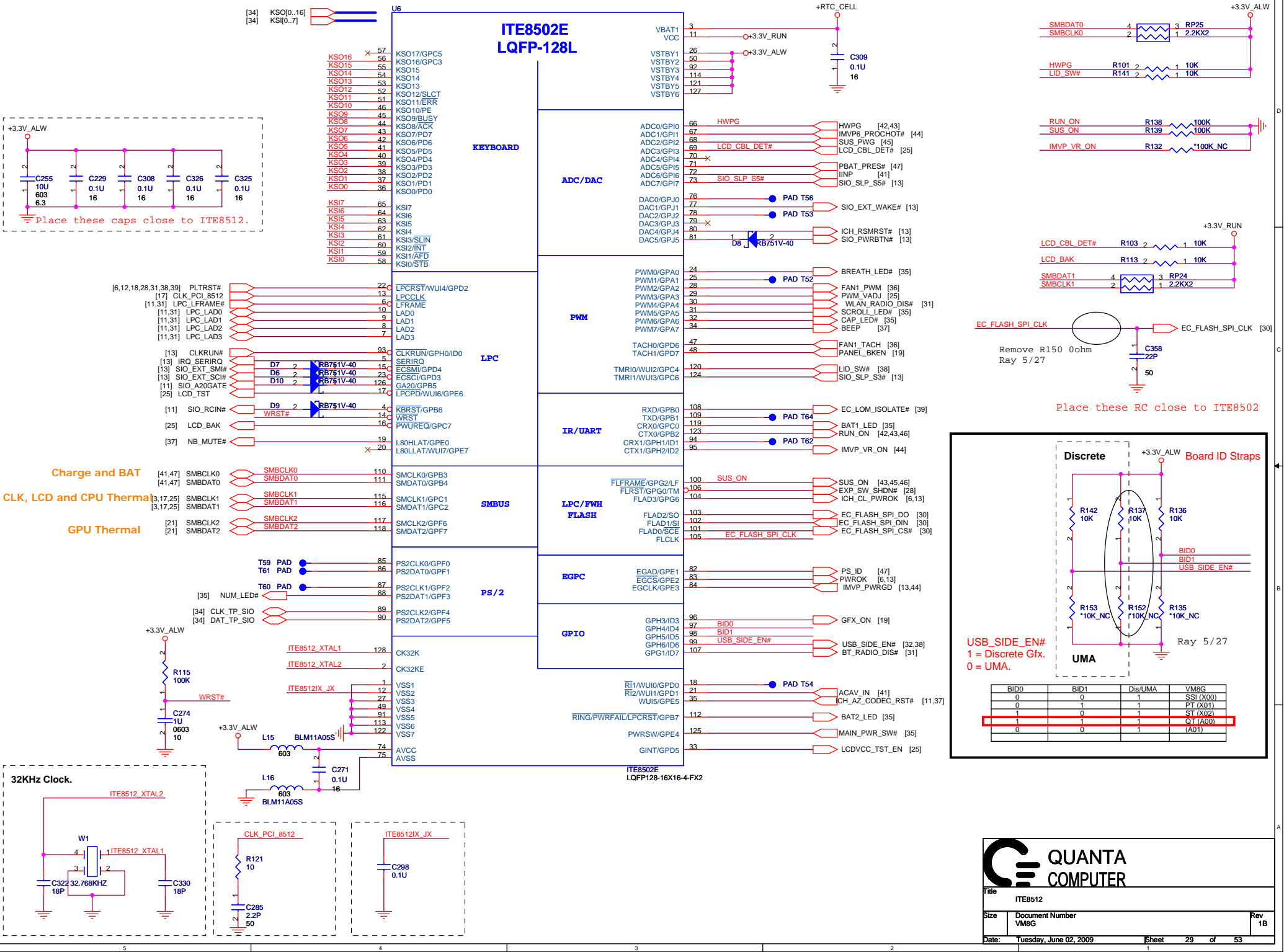
Sheet 27 of 53



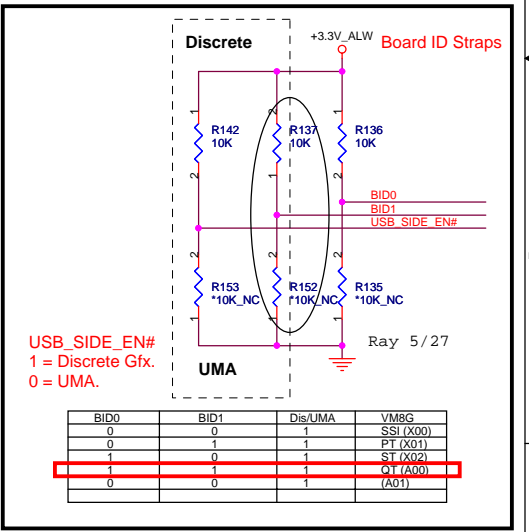
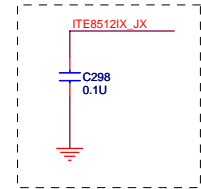
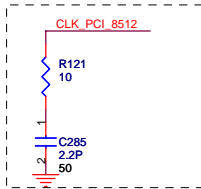
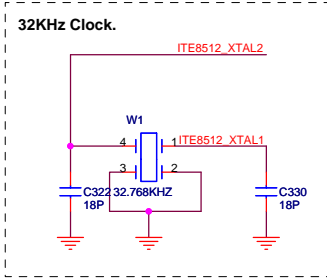
Express Card



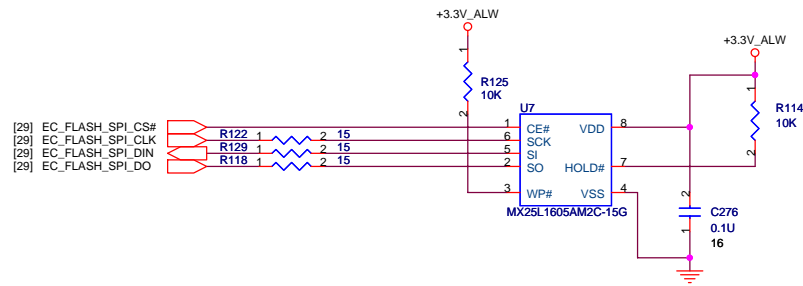
*Express Card cage



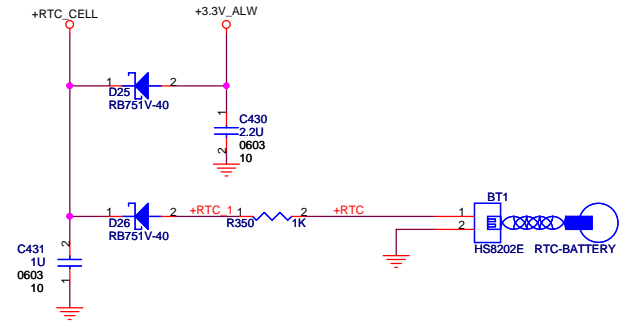
Charge and BAT
CLK, LCD and CPU Thermal
GPU Thermal



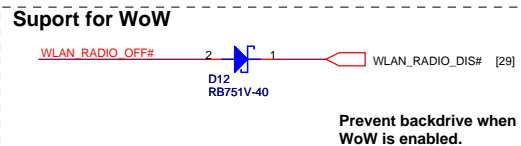
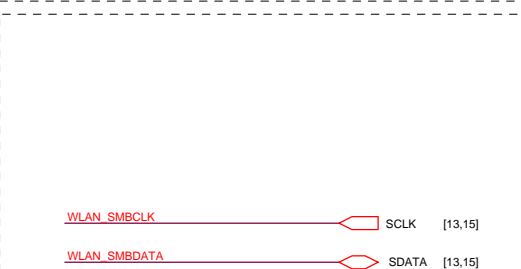
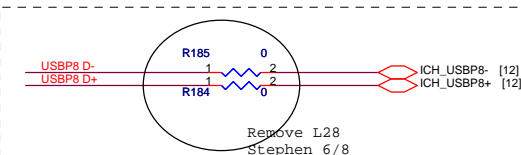
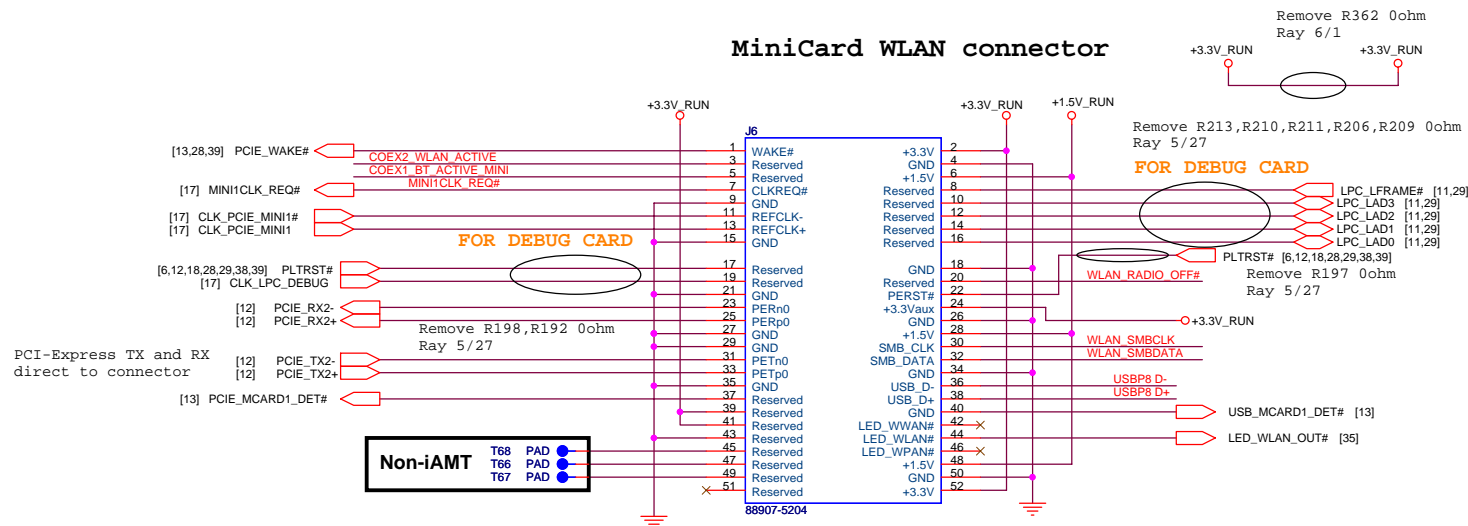
16Mbit (2M Byte), SPI



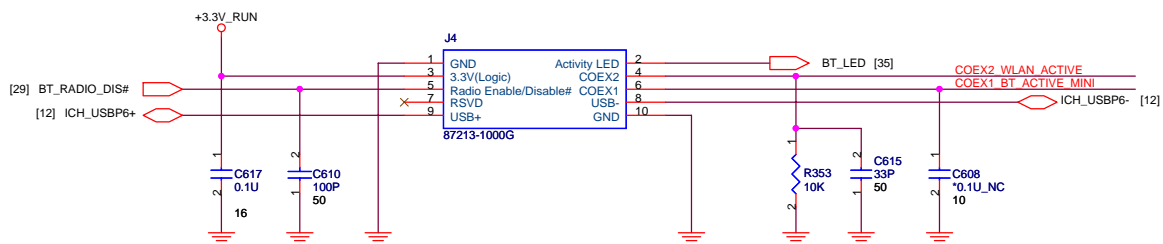
RTC BATTERY



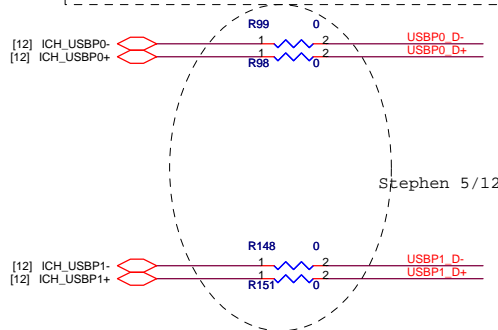
MiniCard WLAN connector



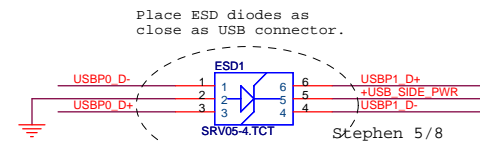
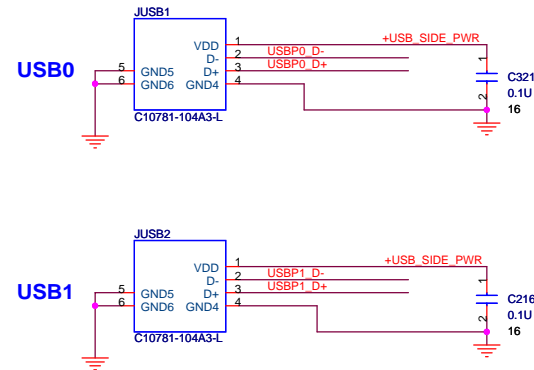
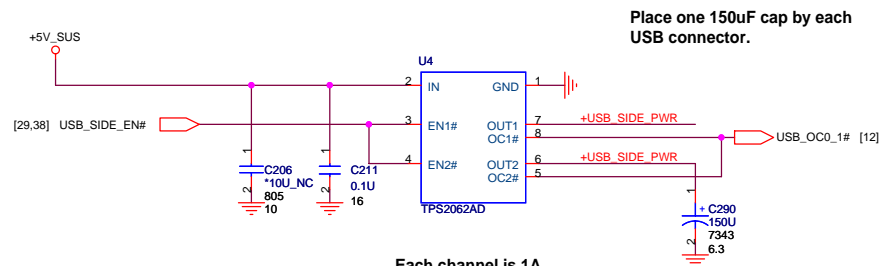
Bluetooth



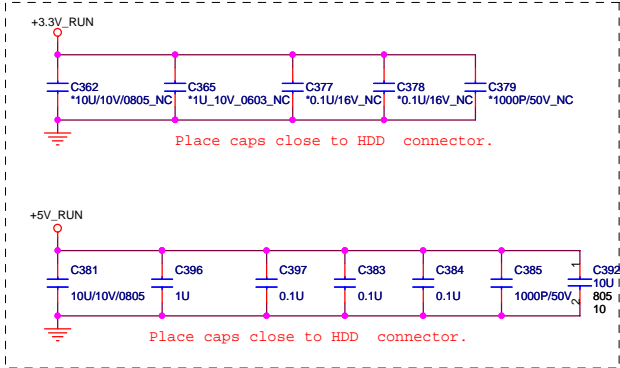
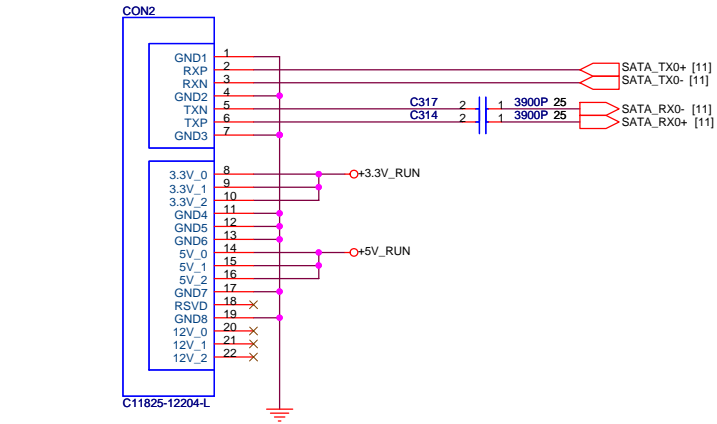
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



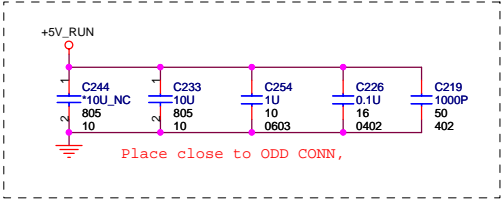
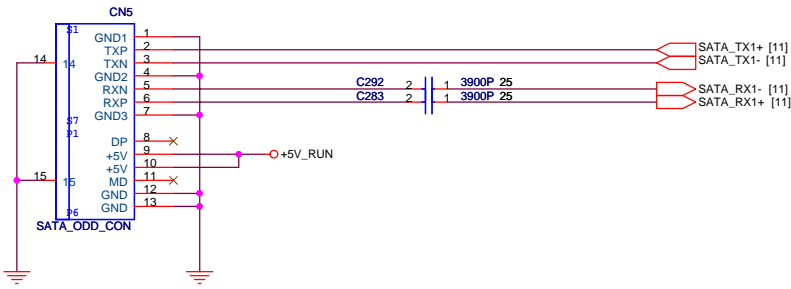
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



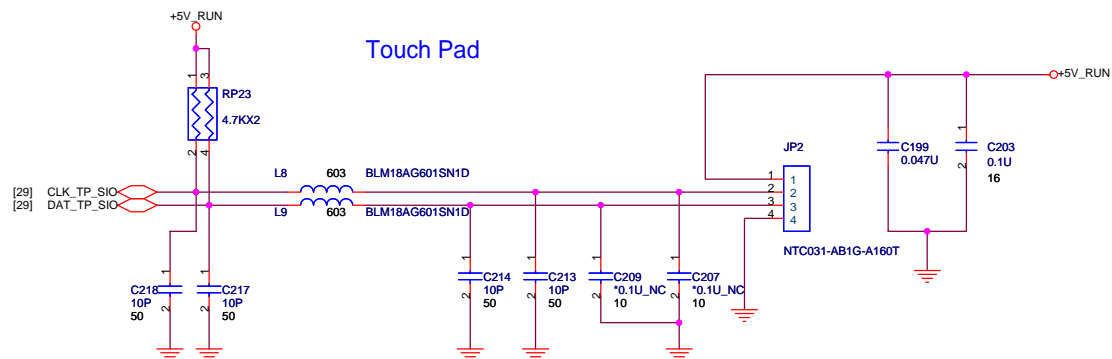
SATA HDD Connector.



SATA ODD Connector.



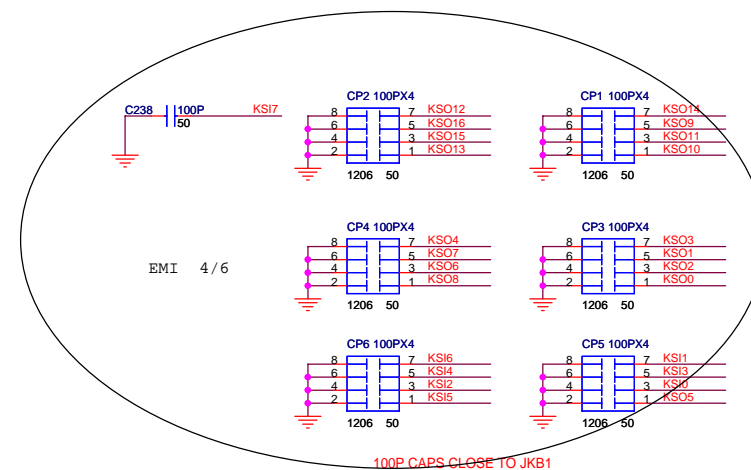
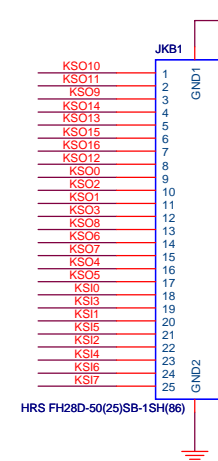
Touch Pad



KEYBOARD CONNECTOR

[29] KSO[0..16]

[29] KSI[0..7]



QUANTA
COMPUTER

Title TOUCH PAD, BULE TOOTH & FIR

Size Document Number VM8G

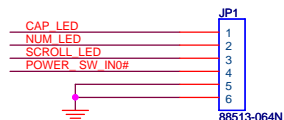
Date: Tuesday, June 02, 2009

Sheet 34 of 53

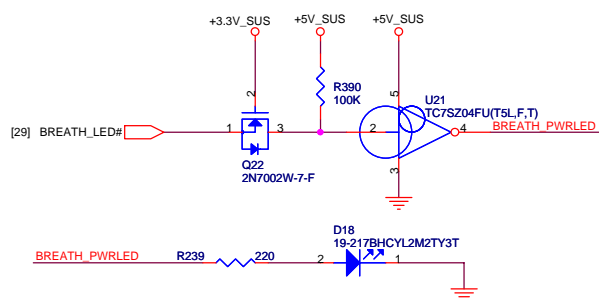
Rev 1B

Keyboard LED

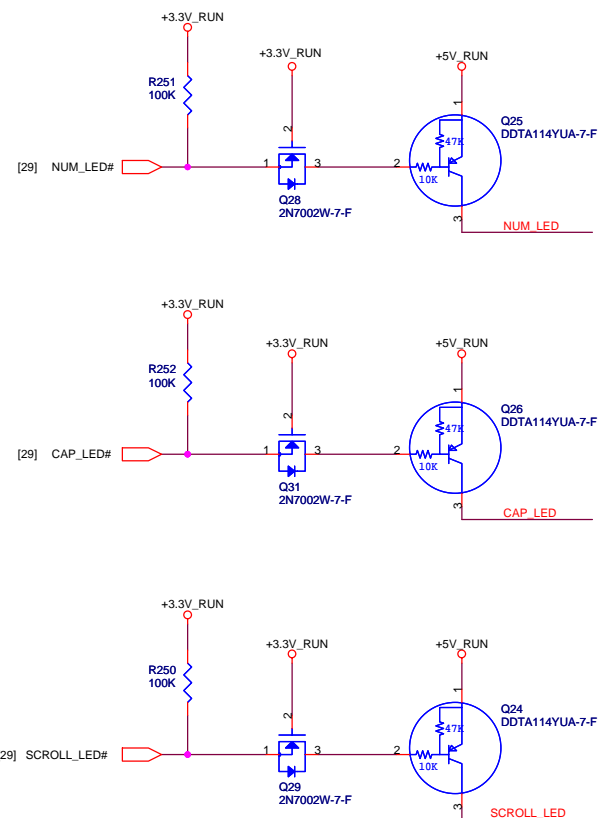
Dash board connector



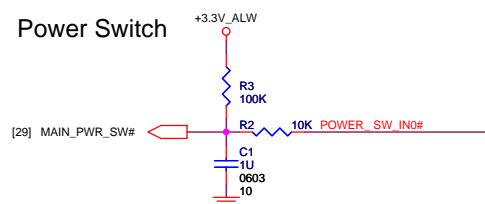
Power & Suspend.



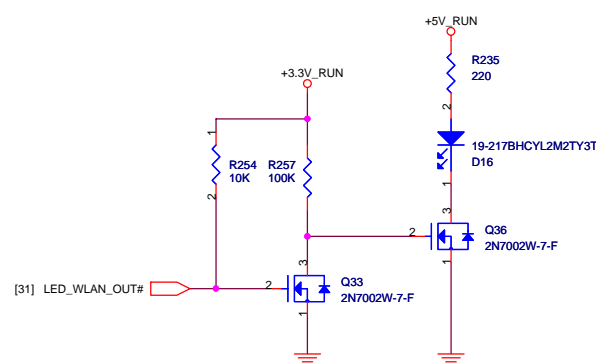
Keyboard LED



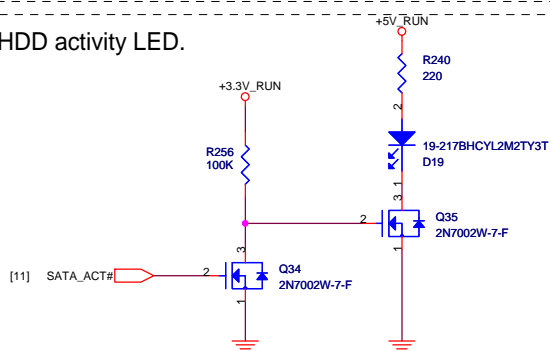
Power Switch



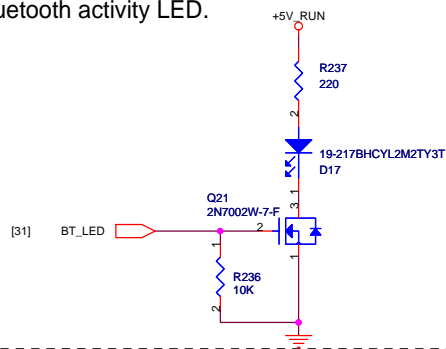
WLAN



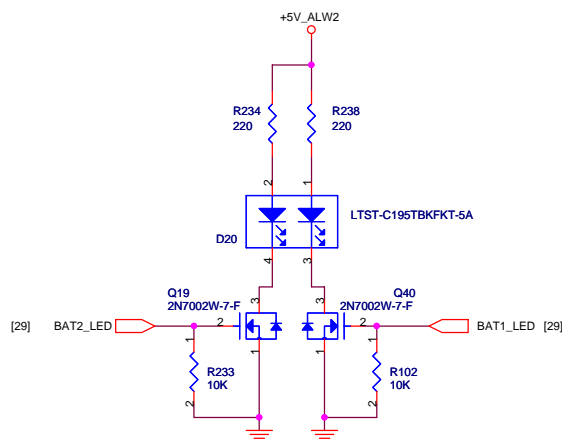
HDD activity LED.



Bluetooth activity LED.



Battery status.



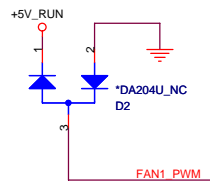
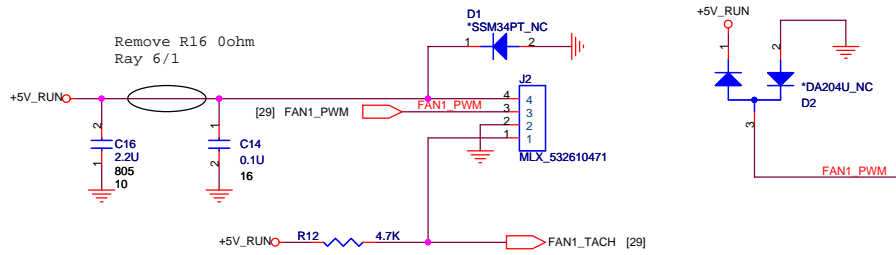
Title SWITCH, KEYBOARD & LED

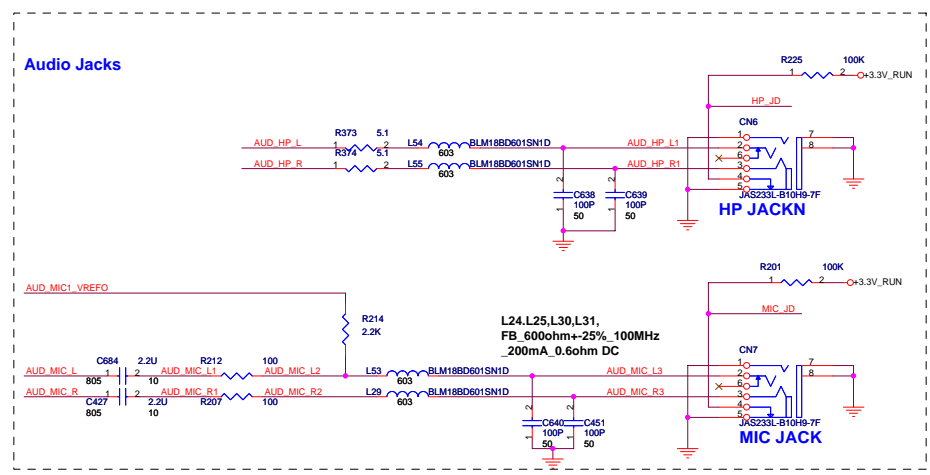
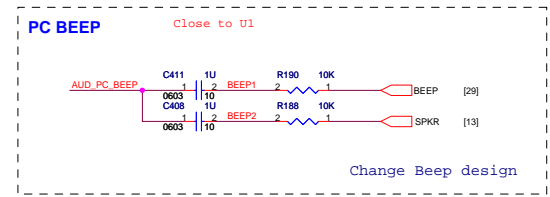
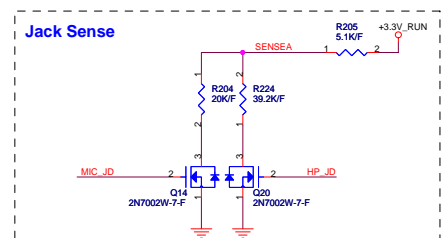
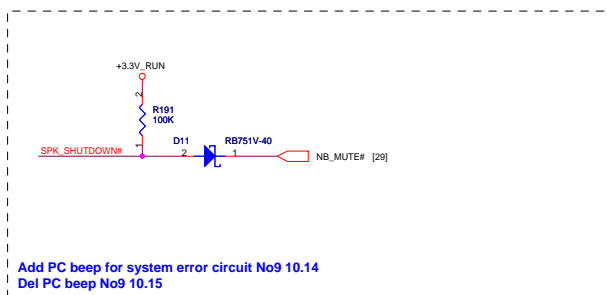
Size	Document Number VM8G
------	-------------------------

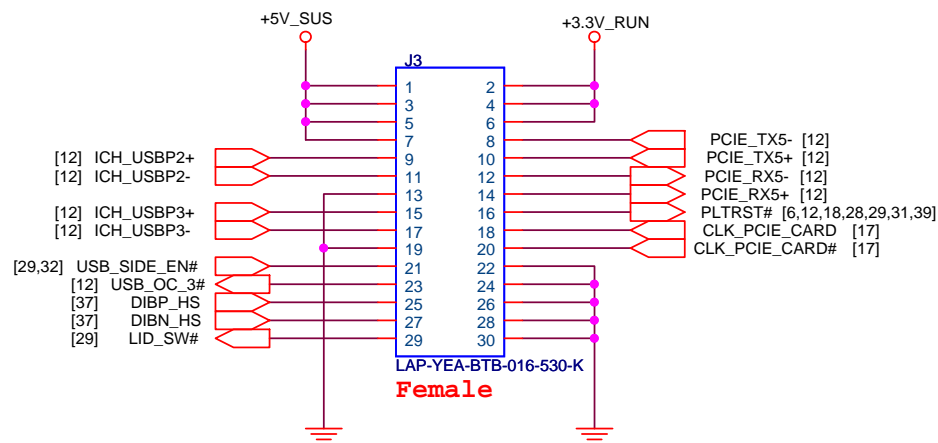
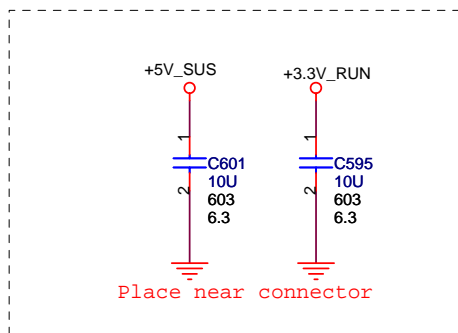
Date: Tuesday, June 02, 2009

Sheet 35 of 53

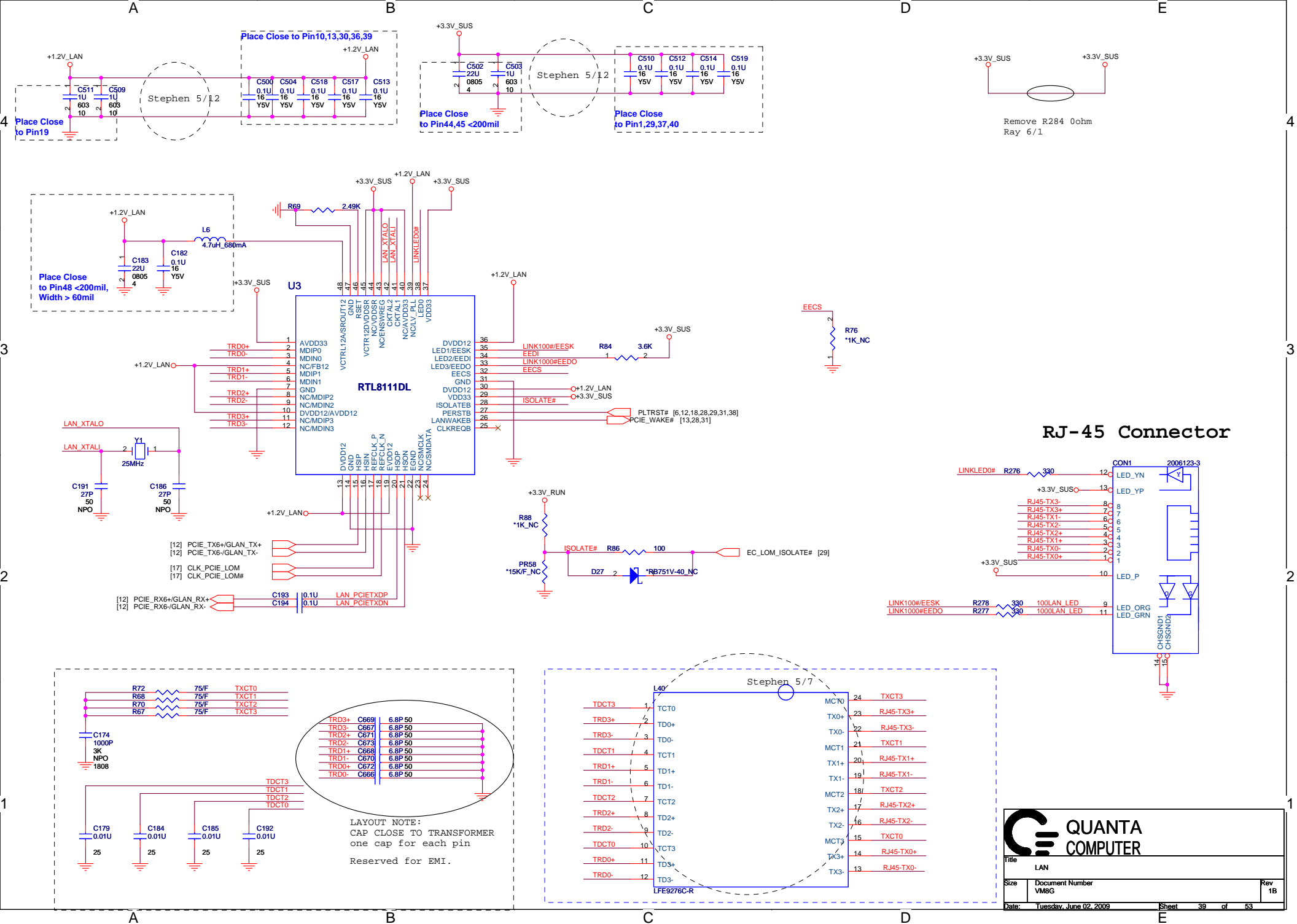
Rev	1B
-----	----

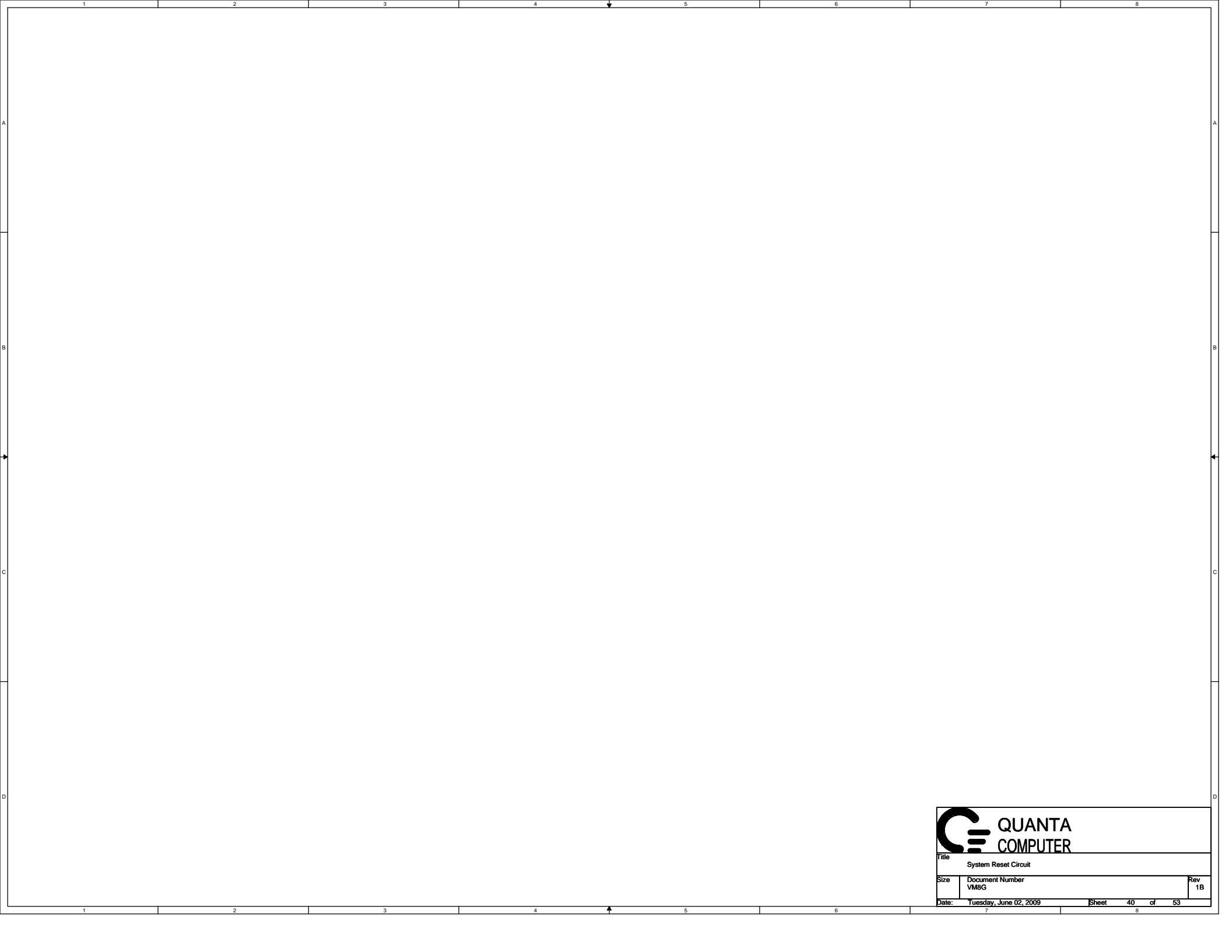







Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)





		QUANTA COMPUTER	
Title System Reset Circuit			
Size	Document Number VM8G		Rev 1B
Date:	Tuesday, June 02, 2009	Sheet 40 of 53	

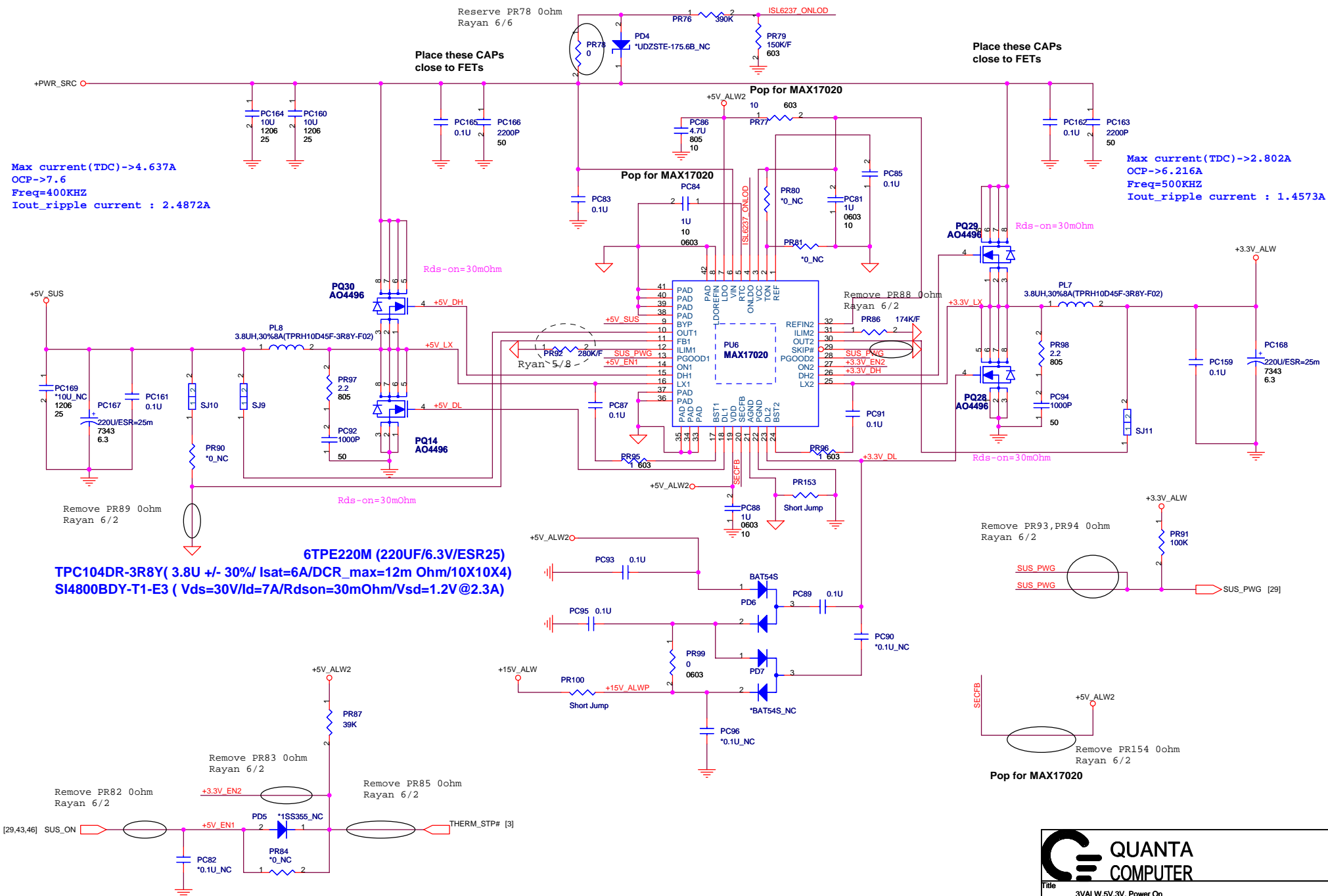
Reserve PR78 0ohm
Rayan 6/6

**Place these CAPs
close to FETs**

**Place these CAPs
close to FETs**

Max current(TDC)->4.637A
OCP->7.6
Freq=400KHZ
Iout_ripple current : 2.4872A

Max current(TDC)->2.802A
OCP->6.216A
Freq=500KHZ
Iout_ripple current : 1.4573A



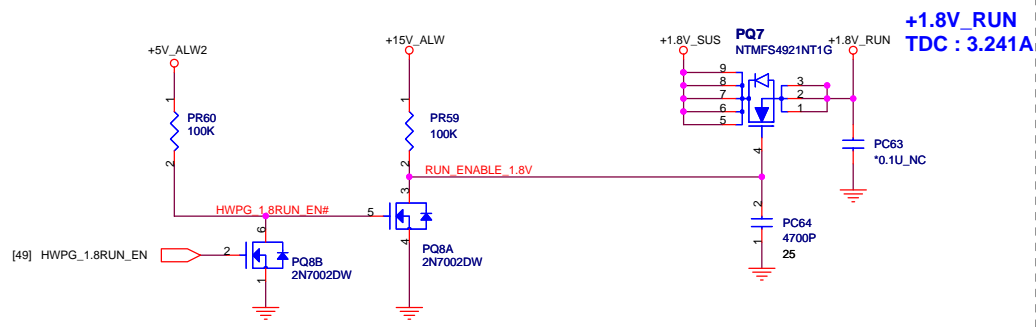
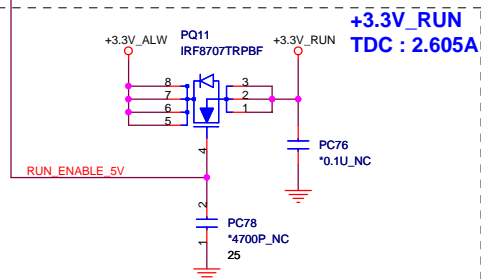
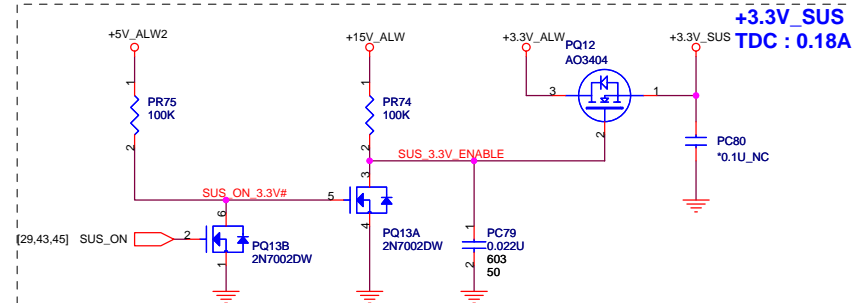
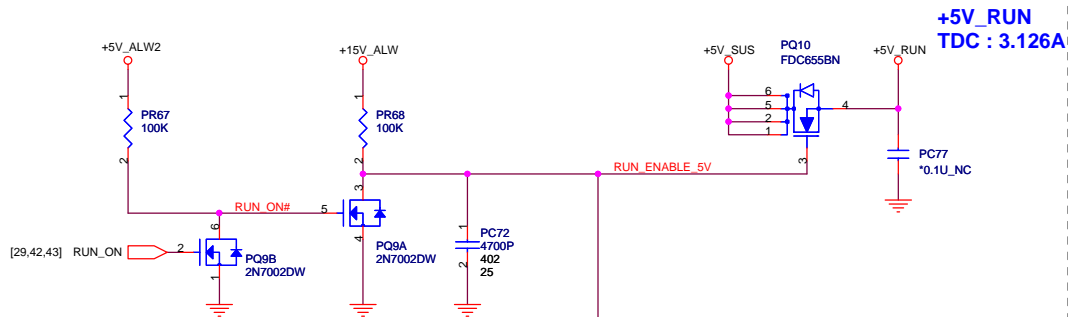
Title 3VALW,5V,3V, Power On

Size	Document Number VM8G
------	-------------------------

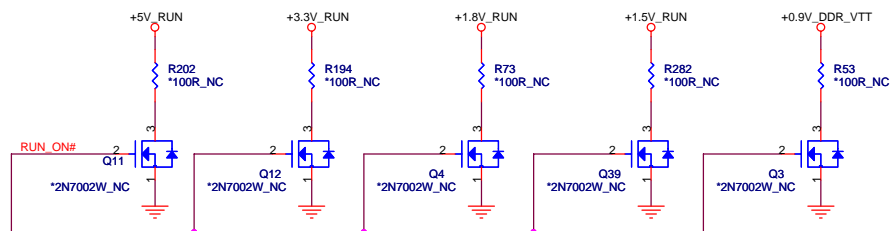
Date: Saturday, June 06, 2009

Sheet 45 of 53

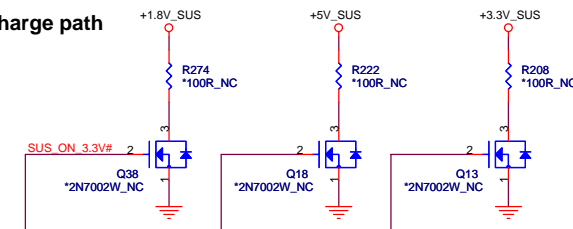
Rev
1B



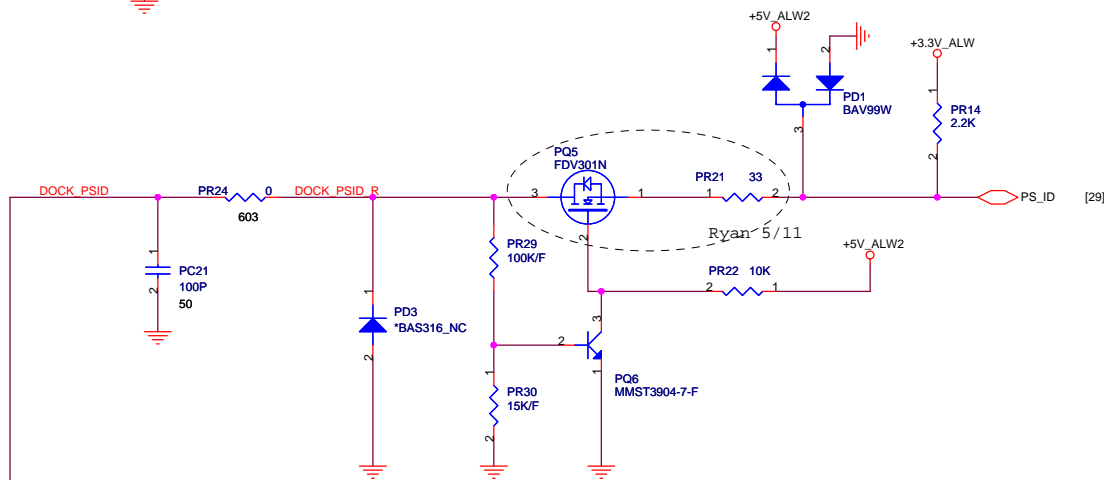
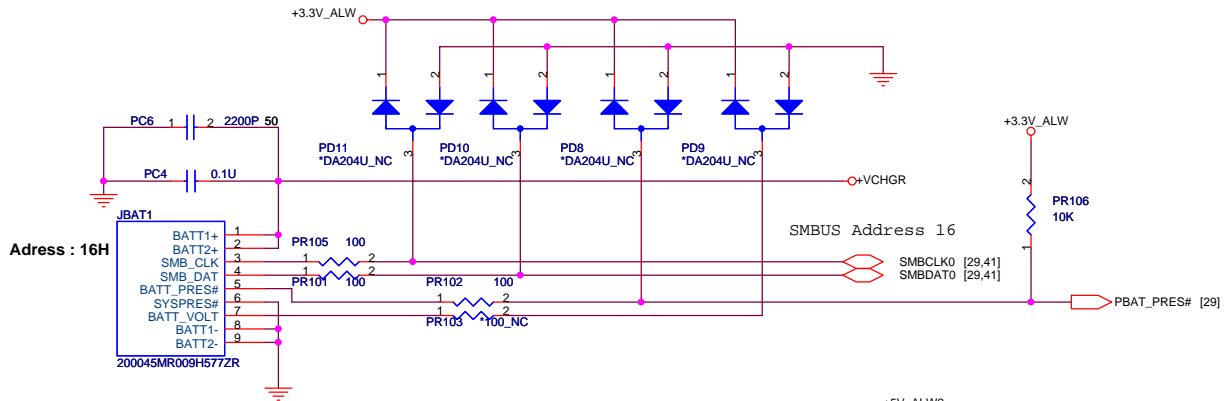
Reserve discharge path



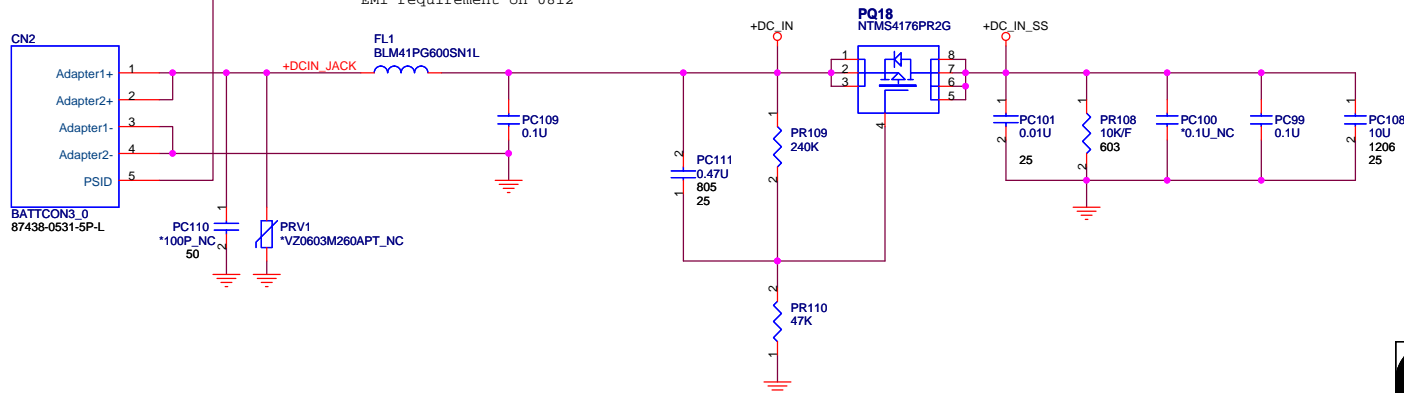
Reserve discharge path



File			RUN POWER SW
Size	Document Number	Rev	
	VM8G	1B	
Date:	Tuesday, June 02, 2009	Sheet	46 of 53



Change Value per GG updated
EMI requirement on 0812



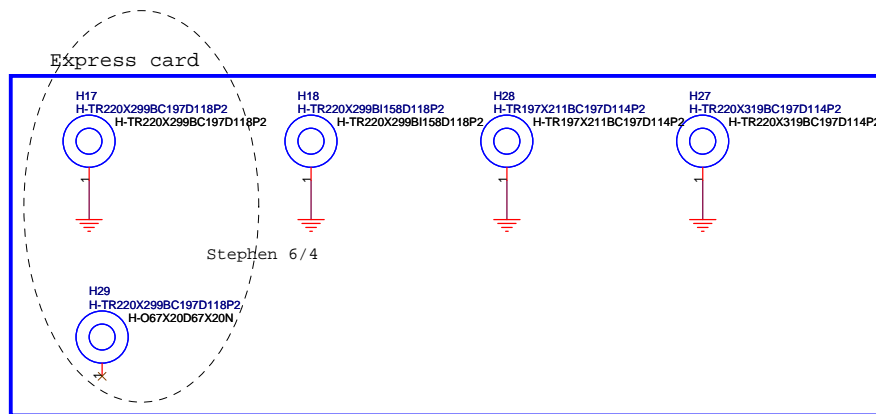
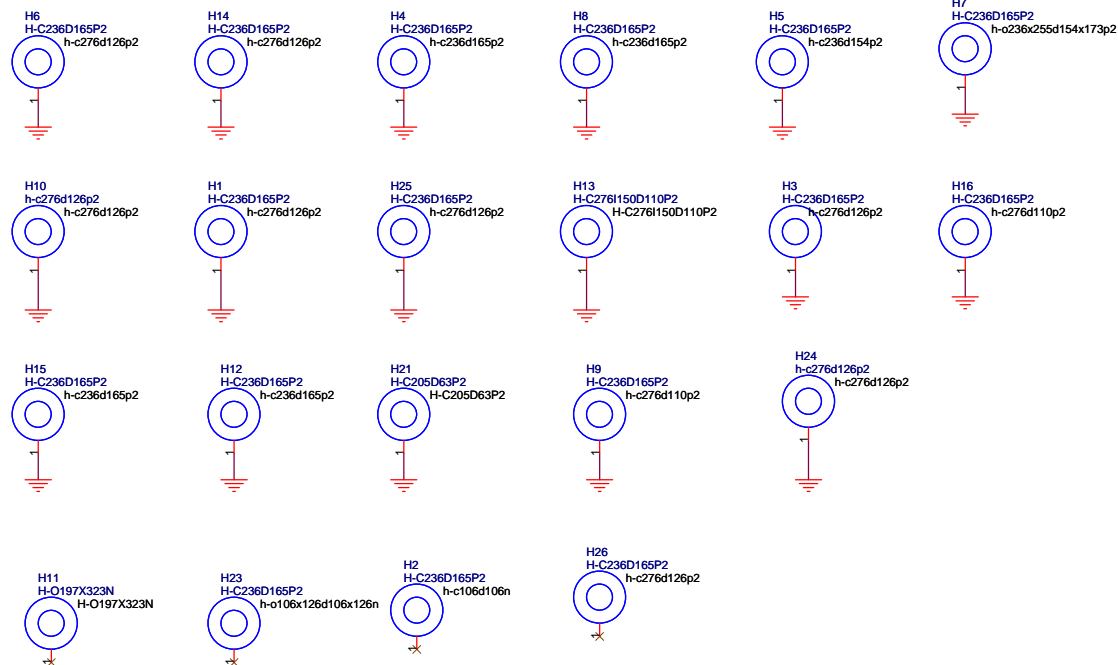
Title
DCIN, BATT CONNECTOR

Size
Document Number
VM8G

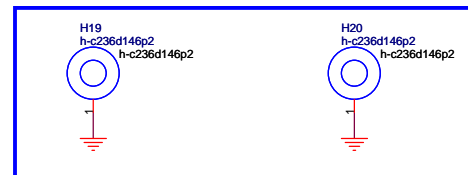
Rev
1B

Date: Tuesday, June 02, 2009

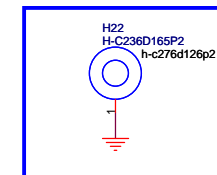
Sheet 47 of 53




DB board



Mini card

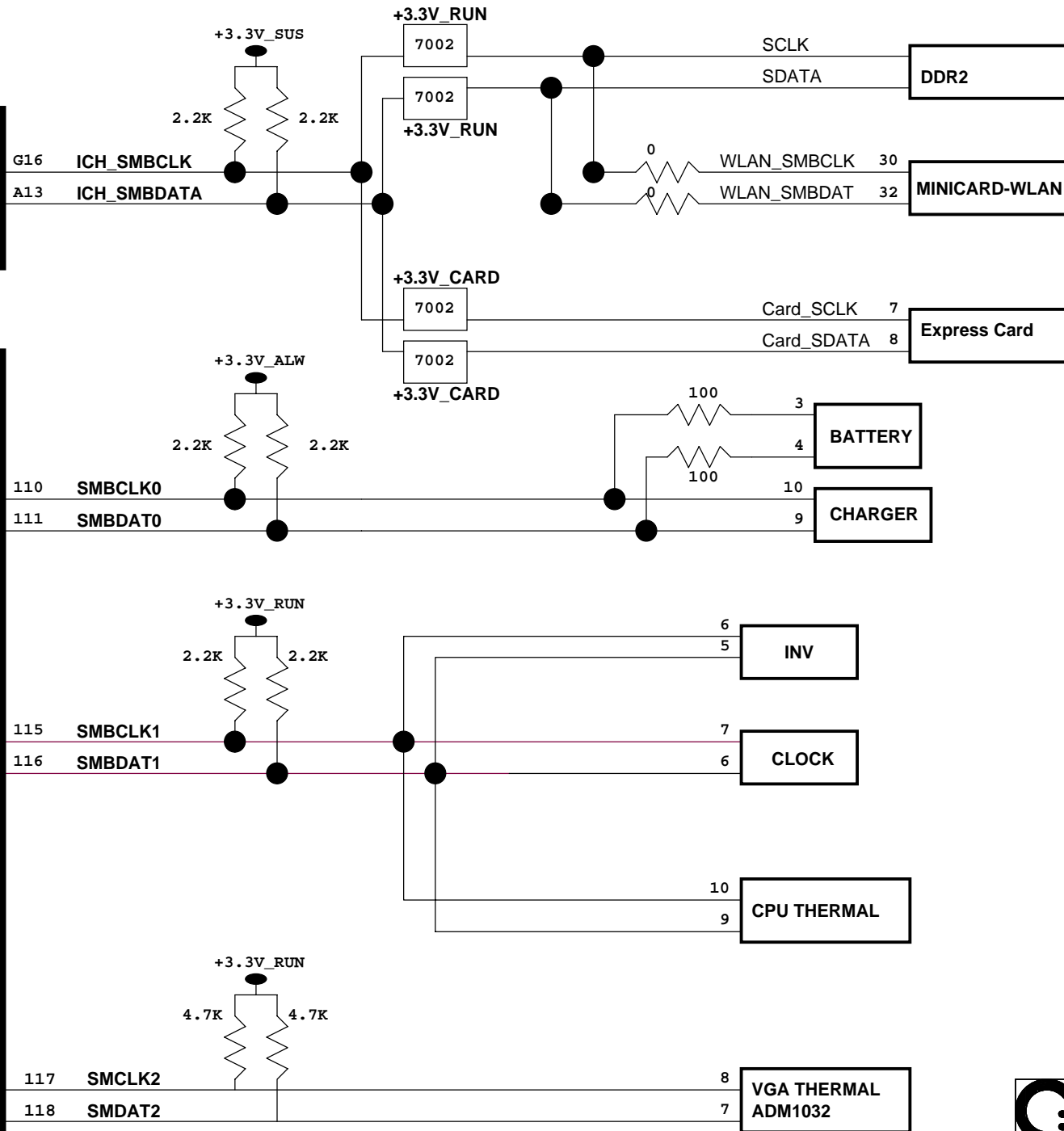


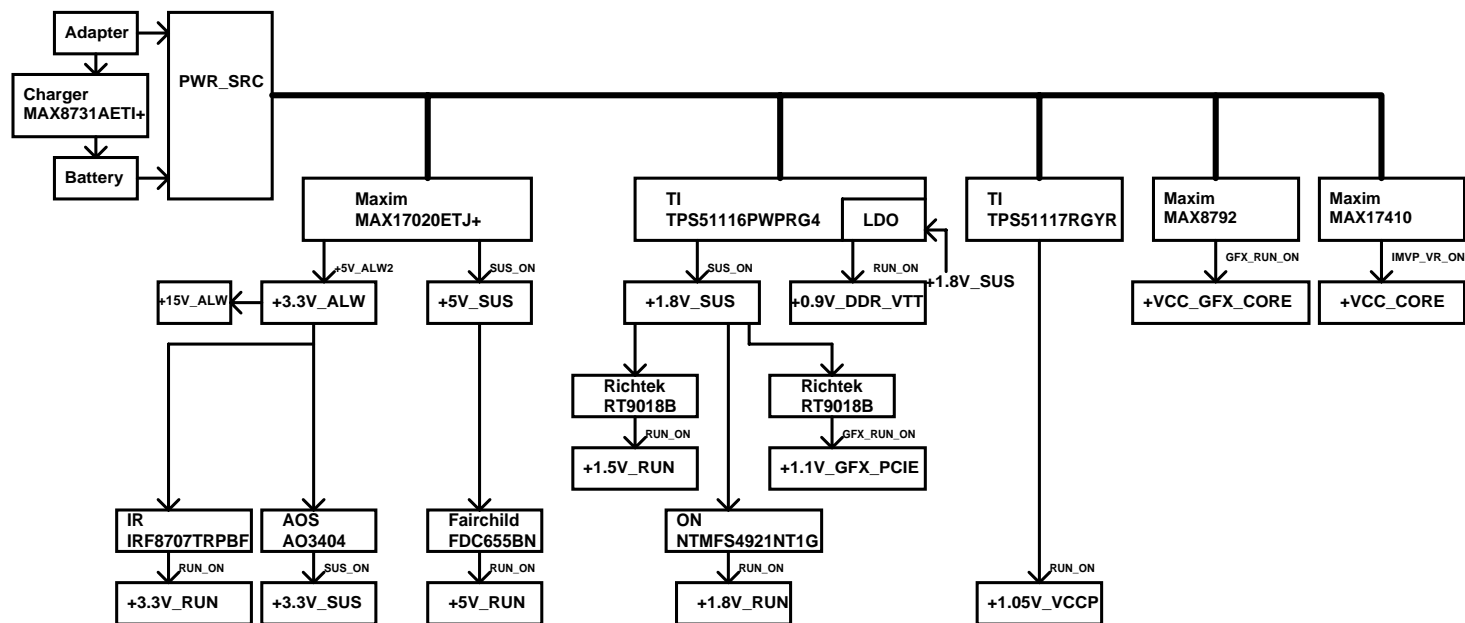
Reserved for EMI.



QUANTA
COMPUTER

Title			
EMI CAP			
Size	Document Number		Rev
	VM8G		1B
Date:	Tuesday, June 02, 2009		Sheet 50 of 53





Power Block Diagram

Size	Document Number VM8G	Rev 1B
------	-------------------------	-----------

Date: Tuesday, June 02, 2009	Sheet 52 of 53
------------------------------	----------------